TOSHIBA Preliminarv

TOSHIBA CCD Linear Image Sensor CCD (charge coupled device)

TCD2916BFG

The TCD2916BFG is a high sensitive and low dark current 10680 elements \times 3 line CCD color image sensor with 10680 elements × 1 line CCD B/W image sensor. The sensor is designed for scanner.

The device contains a row of 10680 elements \times 4 line photodiodes which provide a 48 lines/mm (1200 dpi) across a A4 size paper. The device is operated by 5.0 V pulse and 12 V power supply.



Features

Number of Image Sensing Elements: 10680 elements × 3 line for Color

10680 elements $\times 1$ line for B/W

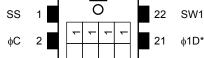
- Image Sensing Element Size: 2.625 µm by 8.4 µm on 2.625 µm centers for Color
- 2.625 µm by 8.4 µm on 2.625 µm centers for B/W
- Photo Sensing Region: High sensitive and low dark current PN photodiode
- Distanced Between Photodiode Array: 31.5 µm (12 lines) R array G array, G array B array

63 µm (24 lines) B array – B/W array

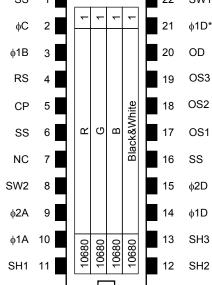
- Clock: 2 phase (5.0 V)
- Power Supply:12 V Power Supply Voltage
- Internal Circuit: Clamp Circuit
- Package: 22 pin CLCC Package
- Color Filter: Red, Green, Blue

Maximum Ratings (Note1)

Characteristic	Symbol	Rating	Unit
Clock pulse voltage	V _φ		
Shift pulse voltage	V _{SH}		
Reset pulse voltage	V _{RS}	-0.3~8.0	V
Clamp pulse voltage	V _{CP}		
Switch pulse voltage	V _{SW}		
Power supply voltage	V _{OD}	-0.3~15	V
Operating temperature	T _{opr}	0~60	°C
Storage temperature	T _{stg}	-25~85	°C



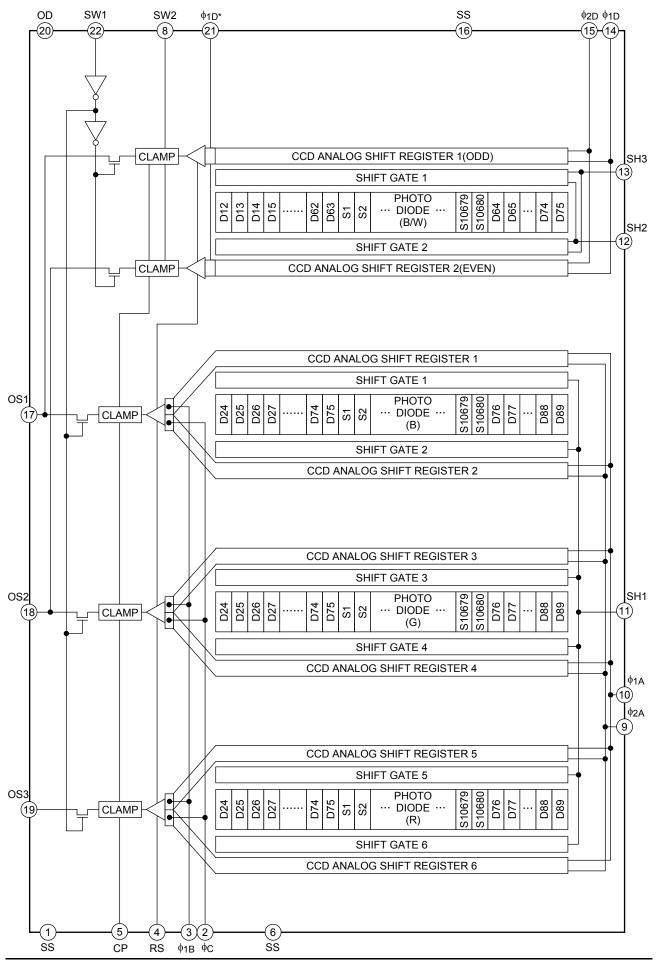
Pin Connections (top view)



Note 1: All voltage are with respect to SS terminals (ground).



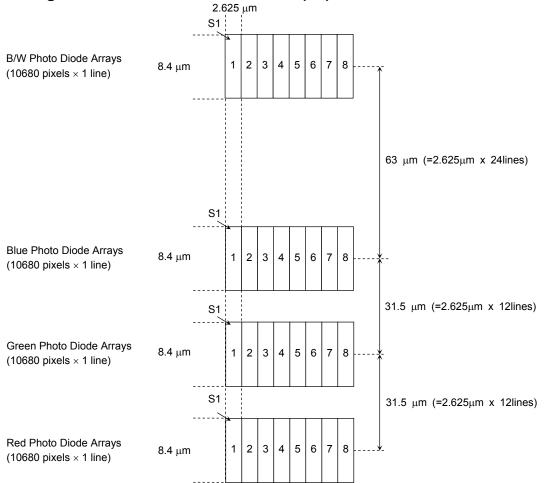
Block Diagram



Pin Names

Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	SS	Ground	22	SW1	Switch Gate 1 for Color or B/W
2	φC	Last stage transfer Clock C for Color	21	φ1D*	Last stage transfer Clock D (phase 1) for B/W
3	φ1B	Last stage transfer Clock B (phase 1) for Color	20	OD	Power
4	RS	Reset Gate	19	OS3	Signal Output 3 (red)
5	СР	Clamp Gate	18	OS2	Signal Output 2 (green or B/W)
6	SS	Ground	17	OS1	Signal Output 1 (blue or B/W)
7	NC	Non Connection	16	SS	Ground
8	SW2	Switch Gate 2 for Hi/Lo amplifier gain for B/W	15	φ2D	Clock D (phase 2) for B/W
9	φ2A	Clock A (phase 2) for Color	14	φ1D	Clock D (phase 1) for B/W
10	φ1A	Clock A (phase 1) for Color	13	SH3	Shift Gate 3 for B/W
11	SH1	Shift Gate 1 for Color	12	SH2	Shift Gate 2 for B/W

Arrangement of The 1st Effective Pixel (S1)



Optical/Electrical Characteristics (Color 1200dpi Mode) (Ta = 25°C, V_{OD} = 12 V, V_{ϕ} = V_{SH} = V_{RS} = V_{CP} = 5.0V (pulse), f_{ϕ} = 2.5 MHz, f_{RS} = 5 MHz, t_{INT} = 11 ms, light source = a light source + CM500S filter (t = 1 mm), load resistance = 100 kΩ)

Characteristics		Symbol	Min	Тур.	Max	Unit	Note
Sensitivity	Red	R (R)	4.6	6.7	8.8		
	Green	R (G)	4.9	7.0	9.1	V/lx∙s	(Note2)
	Blue	R (B)	3.0	4.3	5.6		
Dhoto rooponoo non	uniformity	PRNU (1)	_	10	20	%	(Note3)
Photo response non uniformity		PRNU (3)	_	3	12	mV	(Note4)
Register imbalance	RI	_	1	_	%	(Note5)	
Saturation output vo	V _{SAT}	2.7	3.0	_	V	(Note6)	
Saturation exposure	Saturation exposure		0.29	0.42	_	lx∙s	(Note7)
Dark signal voltage	Dark signal voltage		_	0.2	2.0	mV	(Niete 8)
Dark signal non unif	ormity	DSNU	_	2.7	10.0	mV	(Note8)
DC power dissipatio	n	PD	_	600	780	mW	
Total transfer efficie	ncy	TTE	92	98	_	%	
Output impedance		ZO	Z ₀ — 80 2		250	Ω	
DC output voltage		V _{OS}	5.2	6.6	7.2	V	(Niete())
Reset noise		V _{RSN}	—	0.6	_	V	(Note9)
Random noise		Ν _{Dσ}	—	1.0	_	mV	(Note10)

Optical/Electrical Characteristics (B/W 1200dpi, High Gain Mode) (Ta = 25°C, V_{OD} = 12 V, V_{ϕ} = V_{SH} = V_{RS} = V_{CP} = 5.0 V (pulse), f_{ϕ} = 5 MHz, f_{RS} = 5 MHz, t_{INT} = 11 ms, light source = a light source + CM500S filter (t = 1 mm), load resistance = 100 kΩ)

Characteristics	Symbol	Min	Тур.	Max	Unit	Note
Sensitivity	R (B/W)	16.4	20.6	24.8	V/lx·s	(Note2)
Photo recompany pop uniformity	PRNU (1)	_	10	20	%	(Note3)
Photo response non uniformity	PRNU (3)	_	3	12	mV	(Note4)
Saturation output voltage	V _{SAT}	2.7	3.0	_	V	(Note6)
Saturation exposure	SE	0.10	0.14	_	lx∙s	(Note7)
Dark signal voltage	V _{DRK}	_	0.3	2.0	mV	(Nata 9)
Dark signal non uniformity	DSNU	_	2.7	10.0	mV	(Note8)
DC power dissipation	PD	_	600	780	mW	
Total transfer efficiency	TTE	92	98		%	
Output impedance	ZO	_	80	250	Ω	
DC signal output voltage	V _{OS}	5.2	6.1	7.2	V	(Nata 0)
Reset noise	V _{RSN}	_	0.6	_	V	(Note 9)
Random noise	Ν _{Dσ}	—	1.0		mV	(Note10)

Optical/Electrical Characteristics (B/W 1200dpi, Low Gain Mode) (Ta = 25°C, V_{OD} = 12 V, V_{ϕ} = V_{SH} = V_{RS} = V_{CP} = 5.0 V (pulse), f_{ϕ} = 5 MHz, f_{RS} = 5 MHz, t_{INT} = 11 ms, light source = a light source + CM500S filter (t = 1 mm), load resistance = 100 kΩ)

Characteristics	Symbol	Min	Тур.	Max	Unit	Note
Sensitivity	R _(B/W)	9.9	12.4	14.9	V/lx∙s	(Note2)
	PRNU (1)	_	10	20	%	(Note3)
Photo response non uniformity	PRNU (3)	_	3	12	mV	(Note4)
Saturation output voltage	V _{SAT}	2.7	3.0	_	V	(Note6)
Saturation exposure	SE	0.18	0.24	_	lx∙s	(Note7)
Dark signal voltage	V _{DRK}	_	0.2	2.0	mV	(Nicto 9)
Dark signal non uniformity	DSNU	_	1.5	10.0	mV	(Note8)
DC power dissipation	PD	_	600	780	mW	
Total transfer efficiency	TTE	92	98	_	%	
Output impedance	ZO	_	80	250	Ω	
DC signal output voltage	V _{OS}	5.2	6.2	7.2	V	
Reset noise	V _{RSN}	_	0.5	_	V	(Note 9)
Random noise	N _{Dσ}		0.7		mV	(Note10)

- Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.
- Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

PRNU (1) =
$$\frac{\Delta X}{\overline{X}} \times 100(\%)$$

Where \overline{X} is average of total signal output and ΔX is the maximum deviation from \overline{X} . The amount of incident light is shown below.

 $Red = 1/2 \cdot SE$ Green = 1/2 \cdot SE Blue = 1/4 \cdot SE

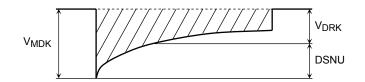
- Note 4: PRNU (3) is defined as maximum voltage with next pixel, where measured approximately 50mV of signal output.
- Note 5: Register imbalance is defined as follows.

$$RI = \frac{\frac{10679}{\sum |Xn-X(n+1)|}}{\frac{n=1}{10679 \times \overline{X}}} \times 100(\%)$$

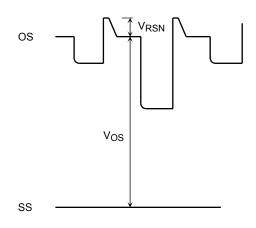
- Note 6: V_{SAT} is defined as minimum saturation output of all effective pixels.
- Note 7: Definition of SE

$$SE_{(B/W)} = \frac{V_{SAT}}{R_{(B/W)}} (Ix \cdot s) \quad SE_{(Color)} = \frac{V_{SAT}}{R_{(G)}} (Ix \cdot s)$$

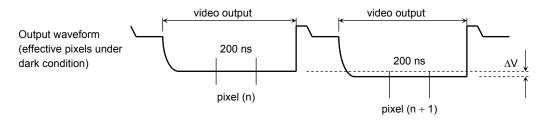
Note 8: V_{DRK} is defined as average dark signal voltage of all effective pixels. DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



Note 9: DC signal output voltage is defined as follows. Reset Noise Voltage is defined as follows.



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



- (1) Two adjacent pixels (pixel n and n + 1) after reference level clamp in one reading are fixed as measurement points.
- (2) Each of the output level at video output periods averaged over 200 ns period to get V (n) and V (n + 1).
- (3) V (n + 1) is subtracted from V (n) to get ΔV .

$$\Delta V = V(n) - V(n+1)$$

(4) The standard deviation of ΔV is calculated after procedure (2) and (3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30} \sum_{i=1}^{30} |\Delta Vi| \qquad \sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (|\Delta V_i| - \overline{\Delta V})^2}$$

- (5) Procedure (2), (3) and (4) are repeated 10 times to get sigma value.
- (6) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

(7) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify random noise as follows.

$$N_{D\sigma} = \frac{1}{\sqrt{2}}\overline{\sigma}$$

Operating Condition

Characteristics	Symbol	Min	Тур.	Max	Unit	
Clock pulse voltage	"H" Level	V _{¢A} , V _{¢D}	4.5	5.0	5.5	V
Clock pulse voltage	"L" Level	ν _φ Α, ν _φ D	0	0	0.5	v
Final Stage Clock voltage	"H" Level		4.5	5.0	5.5	V
Final Stage Clock voltage	"L" Level	· V _{∲1B} , V _{∲C} , V _{∲1D*}	0	0	0.5	v
Shift pulse voltage	"H" Level	V _{SH}	2.7	3.3	5.5	V
	"L" Level	VSH	0	0	0.8	v
Reset pulse voltage	"H" Level	V _{RS}	4.5	5.0	5.5	V
Reset puise voltage	"L" Level	VRS 0		0	0.5	v
Clamp pulse voltage	"H" Level	Vez	4.5	5.0	5.5	V
Clamp pulse voltage	"L" Level	V _{CP}	0	0	0.5	v
Switch pulse voltage	"H" Level	Vou	2.7	3.3	5.5	V
Switch pulse voltage	"L" Level	V _{SW}	0	0	0.8	v
Power supply voltage		V _{OD}	11.4	12.0	12.6	V

Clock Characteristics (Ta = 25°C)

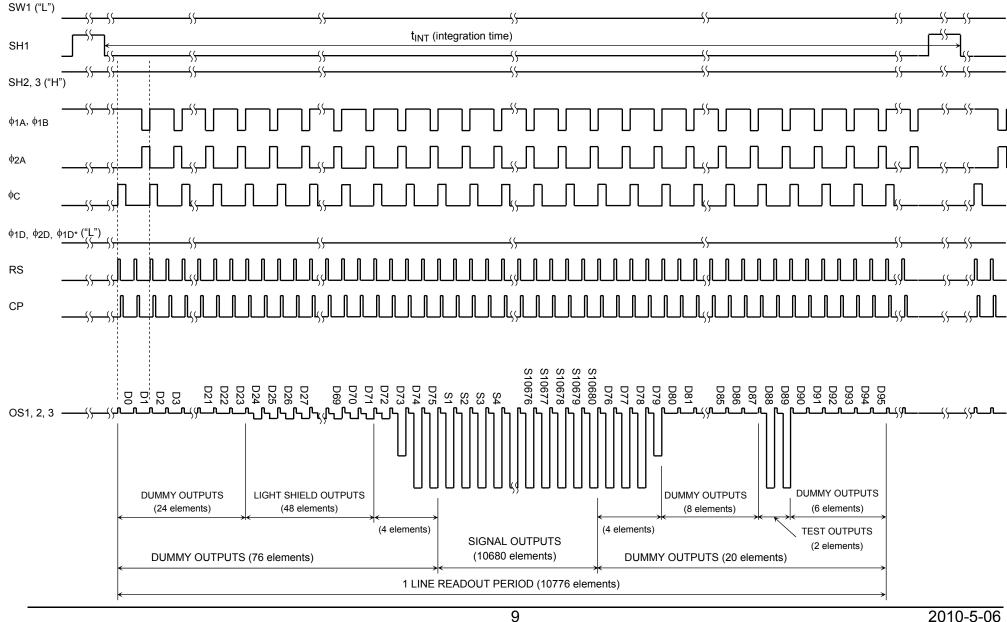
Characteristics	Symbol	Min	Тур.	Max	Unit
Clock pulse frequency	f_{φ}	0.2	5.0	25.0	MHz
Reset pulse frequency	f _{RS}	0.4	5.0	25.0	MHz
Clamp pulse frequency	fCP	0.4	5.0	25.0	MHz
Clock (1A) capacitance for Color (Note 11)	C _{φ1A}	_	265	_	pF
Clock (2A) capacitance for Color (Note 11)	C _{φ2A}	_	270	_	pF
Final Stage Clock capacitance (Note 11)	$C_{\varphi 1B,}C_{\varphi C,}C_{\varphi 1D^{\star}}$	_	6	_	pF
Clock (1D) capacitance for B/W (Note 11)	C _{φ1D}	_	161	—	pF
Clock (2D) capacitance for B/W (Note 11)	C _{¢2D}	_	183	_	pF
Shift gate capacitance	C _{SH}	_	15	_	pF
Reset gate capacitance	C _{RS}		17		pF
Clamp gate capacitance	C _{CP}		11		pF
Switch gate capacitance	C _{SW}		16		pF

Note 11: $V_{OD} = 12 V$

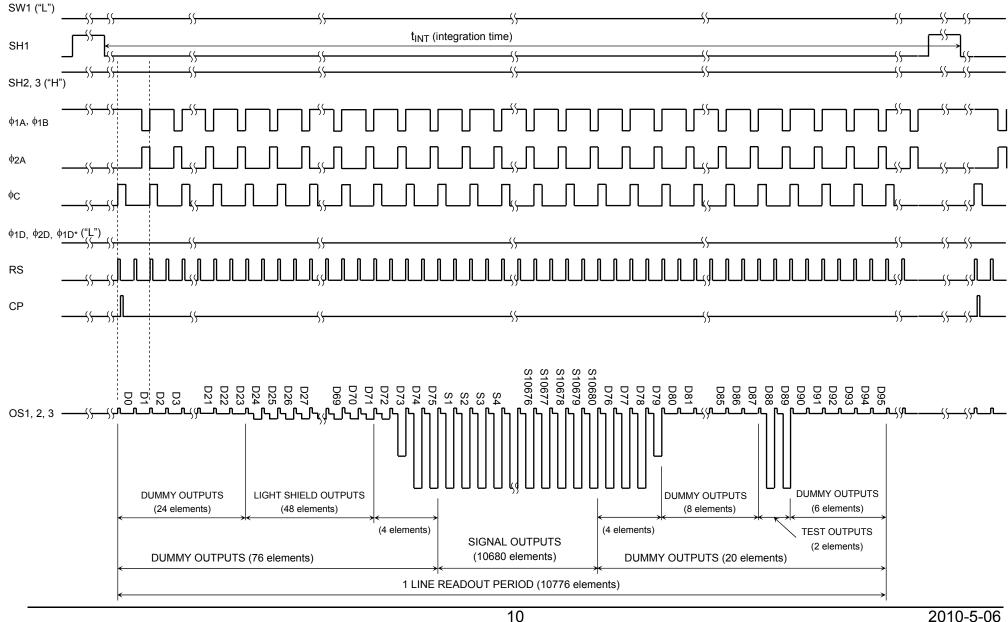
Clocking Mode

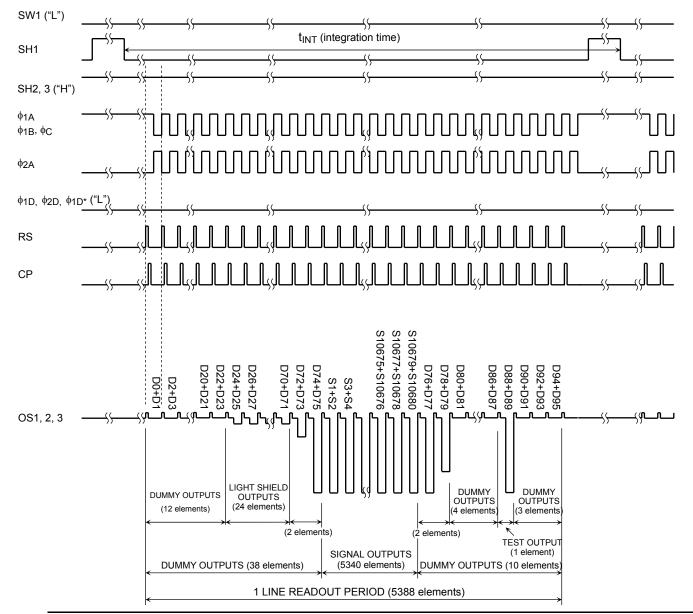
Mode			SW1	SW2	SH1	SH2	SH3	φ1Α, φ2Α	φ1B	φC	φ1D, φ2D	φ1D*	RS	СР								
Bit Clamp	Color 1200DPI 600DPI		"L" "H" P	" L I"	"H" Duloc	"Ц"	"Ц"	"I" "U" Du	"LI" Dulaa	Pulso		H" Pulse	"H" Pulco		- 1"	Pulse	φ1A	Pulse	"I	22	Pulse	Pulse
/ Line Clamp			600DPI	L					i uise	φ1	1A		-	i uise	i uloc							
	B/W High gain		1200DPI	"H" "H"		"H" "H"		Pulse	" "		Pu	lse	Pulse	Pulse								
			600DPI				Pulse			L		Pulse		i uise	i uise							
	B/W Low 12		1200DPI	"[]" "["		"H" "L"		"L" "H" -	Pulse	Pulse	- "L"		Pu	lse	Pulse	Pulse						
В/₩		gain	600DPI		L	Pu	lse			Pu			lse	i uise	i uise							





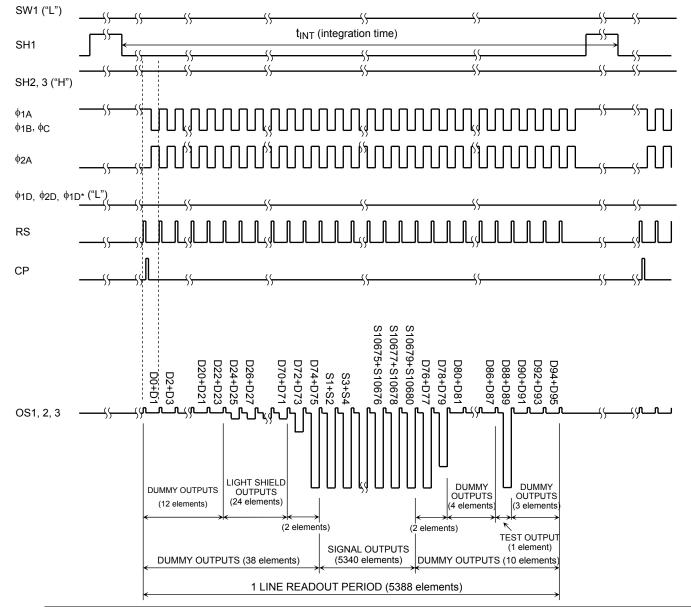




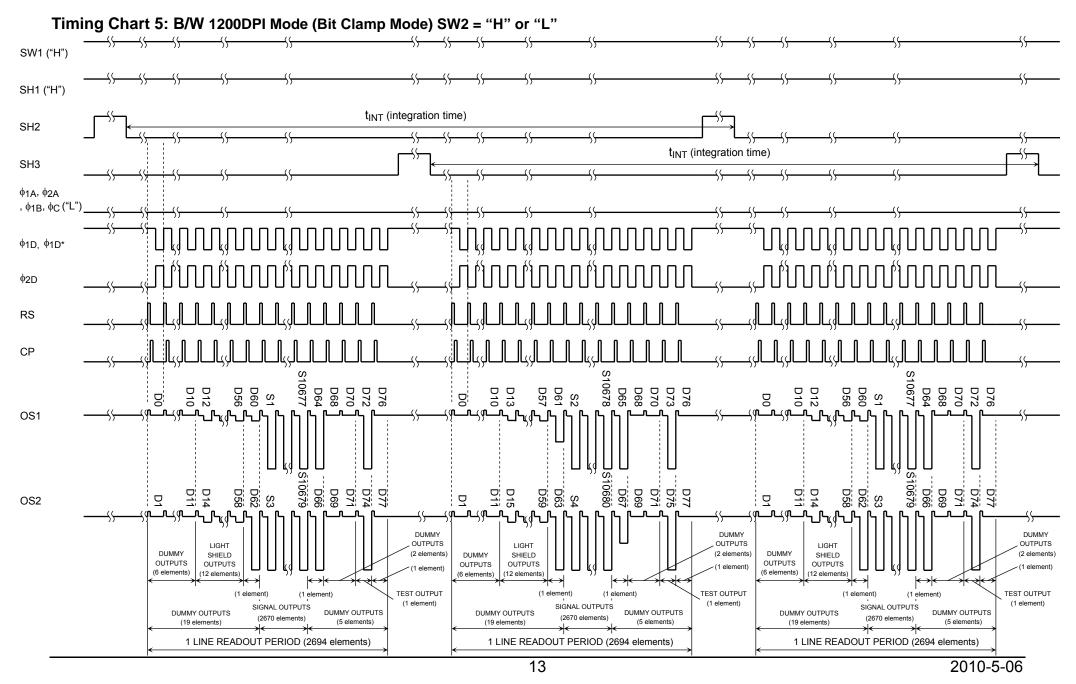


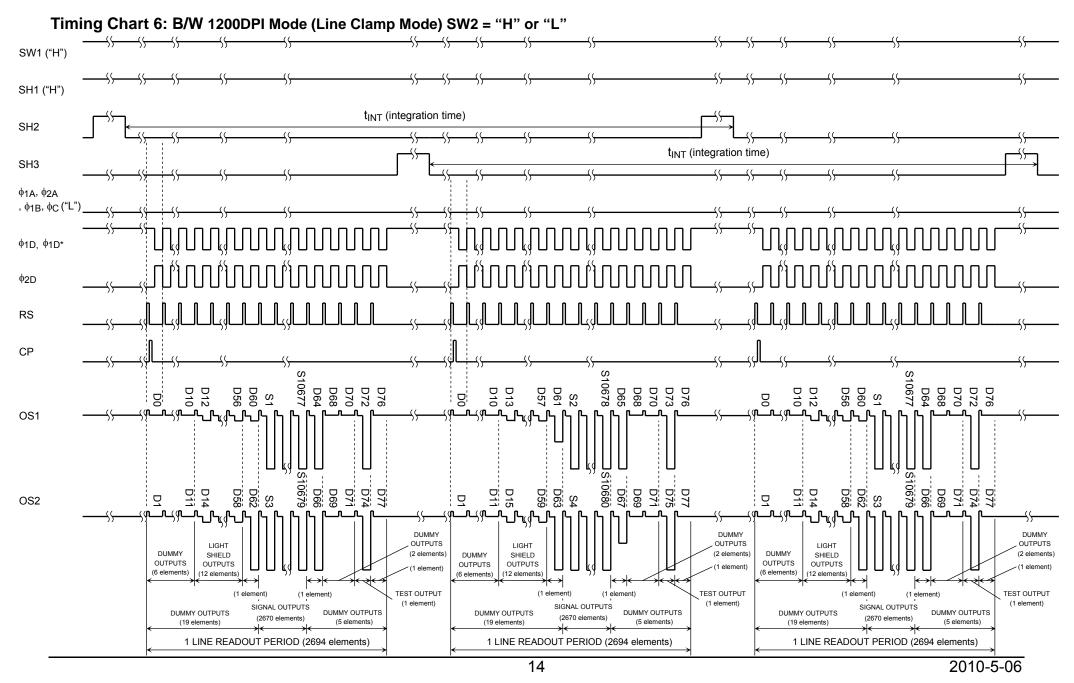
Timing Chart 3: Color 600DPI Mode (Bit Clamp Mode) SW2 = "H"

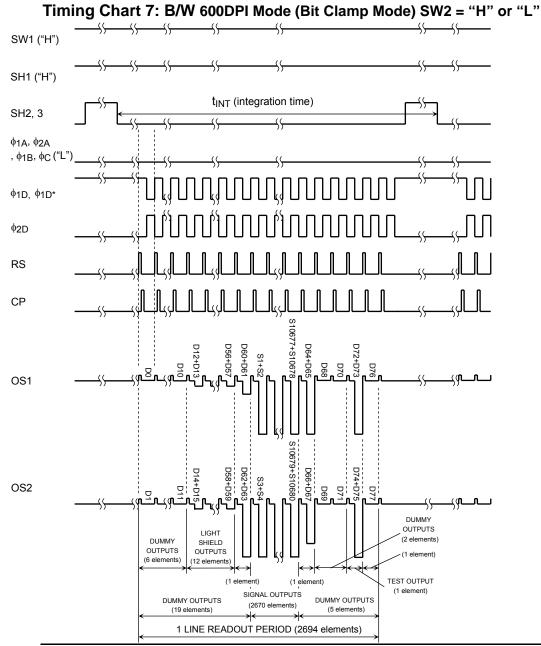
11

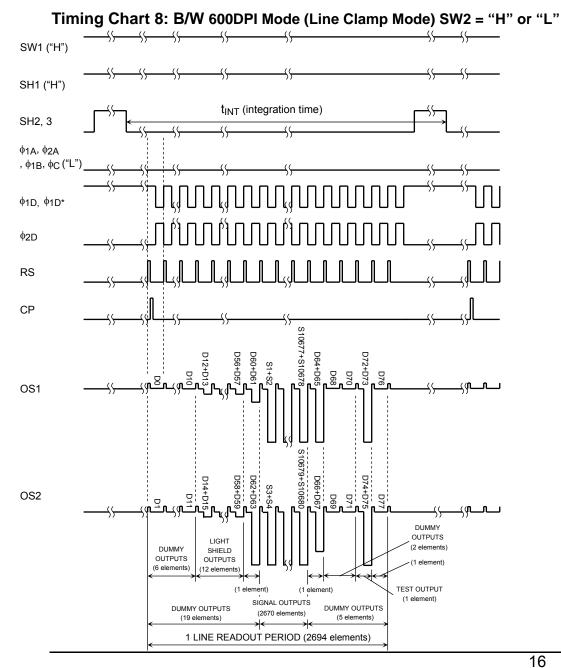


Timing Chart 4: Color 600DPI Mode (Line Clamp Mode) SW2 = "H"









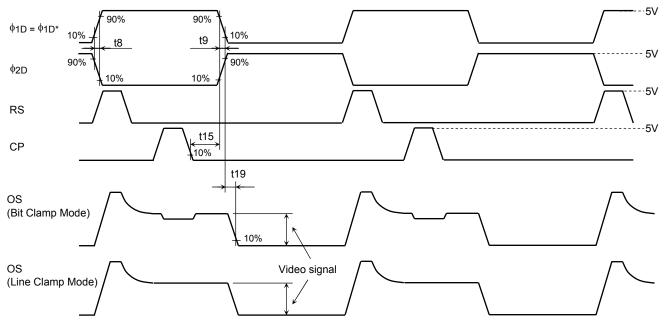
TCD2916BFG

Timing Requirements t3 t4 t2 ---3.3V or 5V t7 t7 90% 90% -4.5V SH φ1 10% 10% -5V 4.0V(min) 4.0V(min) t5 90% t1 90% **¢1** φ2 --0.5V --5V GND t6 RS 3.5 V (max) 10% 1.5 V (min) -----5V (Note12) CP (Note 12) Set the voltage level of RS and CP to "L" level. ---3.3V or 5V t20 SW ("L"→ "H") -----3.3V or 5V SW ("H"→ "L") Color 1200dpi Mode --5V 90% 90% φ1A, φ1B 10% 10% t9 t8 ----- 5V 90% 90% φ2A 10% 10% -•5V 90% 90% φC 10% 10% t10 t11 ---5V 90% 90% RS t12 10% 10% t14 t13 t15 _t15 - t17 t16----·5V 90% 90% CP 10% t18 10% 10% t19 t19 os (Bit Clamp Mode) Video signal Video signal 10% 10% os (Line Clamp Mode) Video signal Video signal Color 600dpi Mode -5V 90% φ1Α, φ1Β, φC 10% ---- 5V 90% φ2A 10% -·5V RS -5V t15 СР 10% t19 os (Bit Clamp Mode) Video signal 10% os (Line Clamp Mode) Video signal

2010-5-06

Timing Requirements (cont.)

B/W 1200dpi Mode & B/W 600dpi Mode (SH2=SH3)



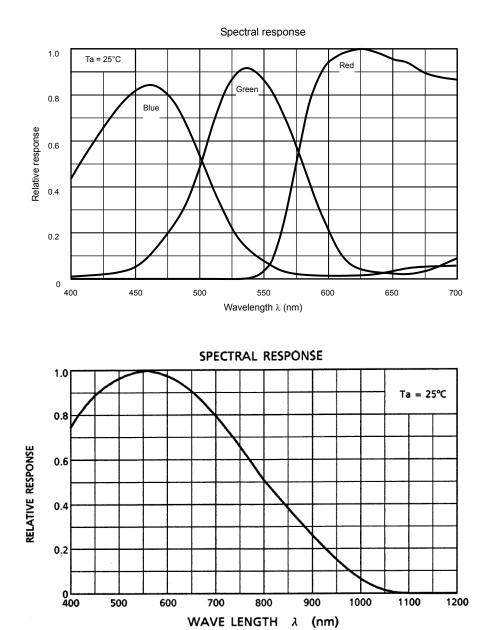
Characteristics	Symbol	Min	Typ. (Note 13)	Max	Unit
Pulse timing of SH and ∳1	t1	120	200	2500	ns
	t5	1000	1075	2500	115
SH pulse rise time, fall time	t2, t4	0	10	_	ns
SH pulse width	t3	3000	3500	_	ns
Pulse timing of SH and RS	t6	975	_	_	ns
φ1A, φ2A pulse width (Note 14)	t7	10	90		20
φ1D, φ2D pulse width (Note 14)		10	90	_	ns
ϕ 1, ϕ 2 pulse rise time, fall time	t8, t9	0	15	_	ns
RS pulse rise time, fall time	t10, t11	0	10	_	ns
RS pulse width	t12	10	15	_	ns
Dulas timing of DS and CD	t13	0	0	_	ns
Pulse timing of RS and CP	t14	10	50	_	ns
Pulse timing of ϕ_{1B} and CP					
Pulse timing of ϕ_{C} and CP	t15	0	40	—	ns
Pulse timing of ϕ_{1D^*} and CP					
CP pulse rise time, fall time	t16, t17	0	10		ns
CP pulse width	t18	10	40		ns
Video data delay time (Note 15)	t19		10		ns
Pulse timing of SH and SW	t20	100	500	t3-100	ns

Note 13: Typ. is the case of f_{RS} = 5.0 MHz.

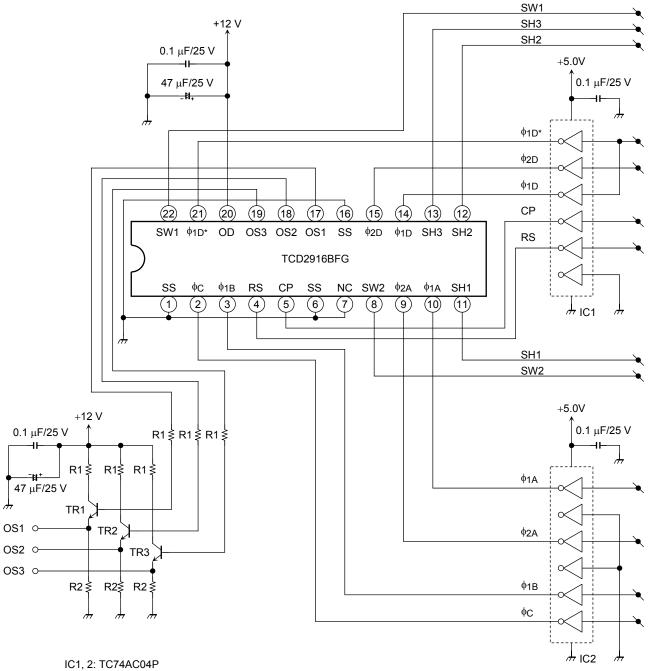
Note 14: Pulse width is the period when voltage difference between $\phi 1$ and $\phi 2$ is over 4.0V. Observe the specification strictly because of normal transfer efficiency.

Note 15: Load Resistance is 100 k Ω .

Typical Spectral Response



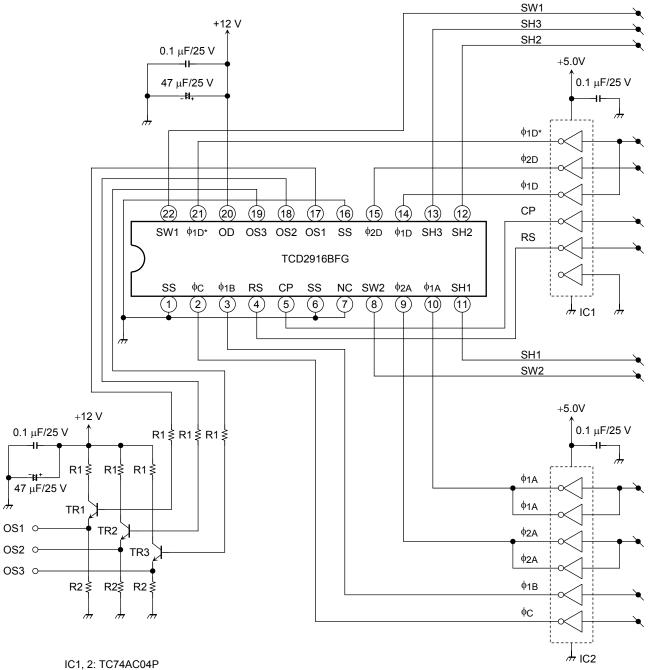
Typical Drive Circuit (at $f\phi=15MHz$ or lower)



TR1, 2, 3: R1: 150 Ω

R2: 1500 Ω

Typical Drive Circuit



TR1, 2, 3: R1: 150 Ω

R2: 1500 Ω

Caution

1. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

CCD Image Sensor is protected against static electricity, but inferior puncture mode device due to static electricity is sometimes detected. In handing the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

- a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
- b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
- c. Ground the tools such as soldering iron, radio cutting pliers of or pincer.It is not necessarily required to execute all precaution items for static electricity.It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.
- d. Ionized air is recommended for discharge when handling CCD image sensors.

2. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

3. Cloudiness of Glass Inside

CCD surface mount products may have a haze on the inside of glass, so be careful about following. Even if the haze arises inside of glass, when it is not on the pixel area, there is no problem in quality. •Before the aluminum bag is opened, please keep the products in the environment below 30°C90%RH. And after the aluminum bag is opened, please keep the products in the environment below 30°C60%RH.

• Please mount the products within 12month from sealed date and within 6 month from opening the aluminum bag. (Sealed date is printed on aluminum bag.)

4. Ultrasonic Cleaning

Ultrasonic cleaning should not be used with such hermetically-sealed ceramic package as CCD because the bonding wires can become disconnected due to resonance during the cleaning process.

5. Mounting

In the case of solder mounting, the devices should be mounted with the window glass protective tape in order to avoid dust or dirt included in reflow machine.

6. Window Glass Protective Tape

The window glass protective tape is manufactured from materials in which static charges tend to build up. When removing the tape from CCD sensor after solder mounting, install an ionizer to prevent the tape from being charged with static electricity.

When the tape is removed, adhesives will remain in the glass surface. Since these adhesives appear as black or white flaws on the image, please wipe the window glass surface with the cloth into which the organic solvent was infiltrated. Then please attach CCD to a product.

Do not reuse the tape.

7. Soldering Temperature Profile for Pb free

Good temperature profile for each soldering method is as follows. In addition, in case of the repair work accompanied by IC removal, since the degree of parallel may be spoiled with the left solder, please do not carry out and in case of the repair work not accompanied by IC removal, carry out with a soldering iron or , in reflow, only one time.

- a. Using a soldering iron Complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.
- b. Using long infrared rays reflow / hot air reflow
 Please do reflow at the condition that the package surface (electrode) temperature is on the solder maker's recommendation profile. And that reflow profile is within below condition 1 to 3.
- 1. Peak temperature: 250°C or less.
- 2. Time to keep high temperature : $220 \sim 250^{\circ}$ C, $30 \sim 40$ sec.
- 3. Pre. heat : 150~190°C, 60~120sec

8. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor. Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

9. Cleaning Method of the Window Glass Surface

Wiping Cloth

- a. Use soft cloth with a fine mesh.
- b. The wiping cloth must not cause dust from itself.
- c. Use a clean wiping cloth necessarily.
- Recommended wiping cloth is as follow;
- MK cloth (Toray Industries)

Cleaner

Recommended cleaning liquid of window glass are as follow;

- EE-3310 (Olympus)

When using solvents, such as alcohol, unavoidably, it is cautious of the next.

- a. A clean thing with quick-drying.
- b. After liquid dries, there needs to be no residual substance.
- c. A thing safe for a human body.

And, please observe the use term of a solvent and use the storage container of a solvent to be clean. Be cautious of fire enough.

Way of Cleaning

First, the surface of window glass is wiped with the wiping cloth into which the cleaner was infiltrated. Please wipe down the surface of window glass at least 2 times or more.

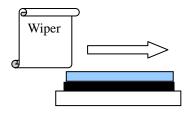
Next, the surface of window glass wipes with the dry wiping cloth. Please wipe down the surface of window glass at least 3 times or more.

Finally, blow cleaning is performed by dry N2 filtered.

If operator wipes the surface of the window glass with the above-mentioned process and dirt still remains, Toshiba recommends repeating the clean operation from the beginning.

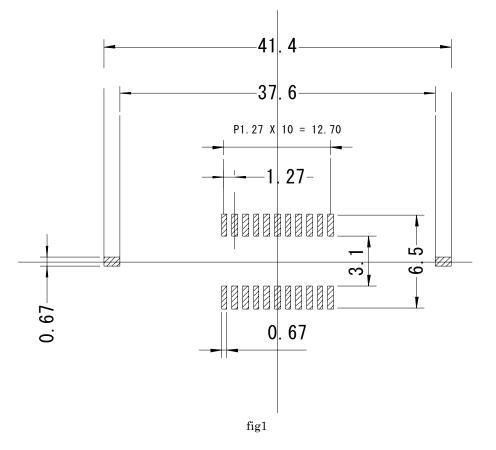
Be cautious of the next thing.

- a. Don't infiltrate the cleaner too much.
- b. A wiping portion is performed into the optical range and don't touch the edge of window glass.
- c. Be sure to wipe in a long direction and the same direction.
- d. A wiping cloth always uses an unused portion.



10. Foot Pattern on the PCB

We recommend fig1 's foot pattern for your PCB(Printed circuit Board).



11. Mask for Solder Paste Application

We recommend metal mask that have the following thickness.

•TCD****BFG(Pad material : Au) : a thickness of 0.2mm.

And we recommend that the size of the pattern of the metal mask is 95% to 100% of recommended foot pattern at fig1.

12. Temperature cycle

After mounting, if temperature cycle stress is too much, CCD surface mount products have a possibility that a crack may arise in solder. As a method of preventing a solder crack, underfil is effective

13. Reuse of a Tray

We reuse tray in order to reduce plastic waste as we can. Please cooperate with us in reusing for ecology.

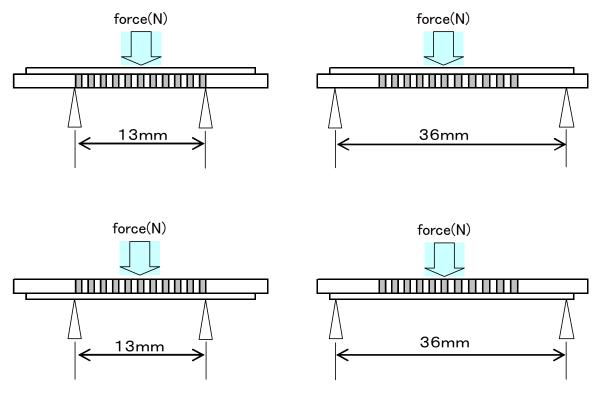
14. Caution for Package Handling

Over force on CCD products may cause crack and chip removing on the product. The three point bending strength of this product is the following. (Reference data)

If the stress is loaded far from a fulcrum, the stress on the package will be increase.

When you will treat CCD on every process, please be careful particularly. For example, soldering on PCB, cutting PCB, wiping on the glass surface, optical assemble and so on.

Bending Test



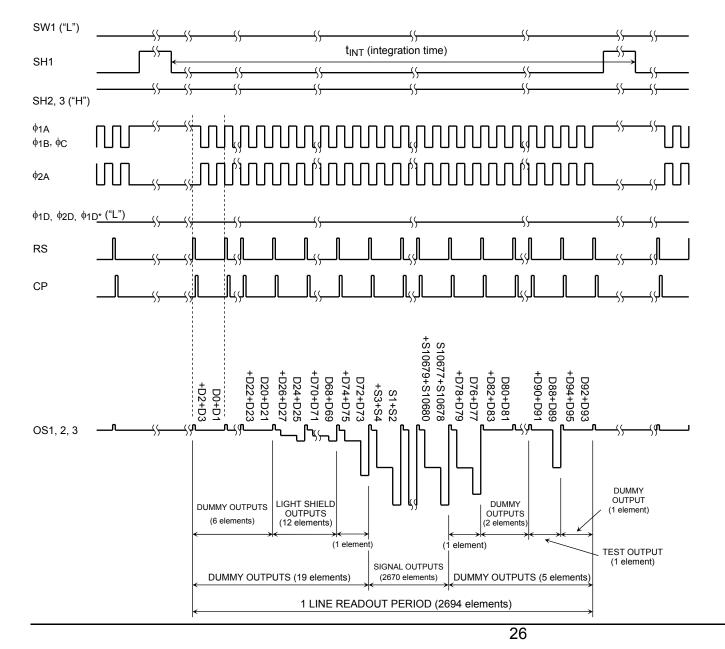
 $\cdot 22 \text{CLCC}$

Bearing length 13mm:

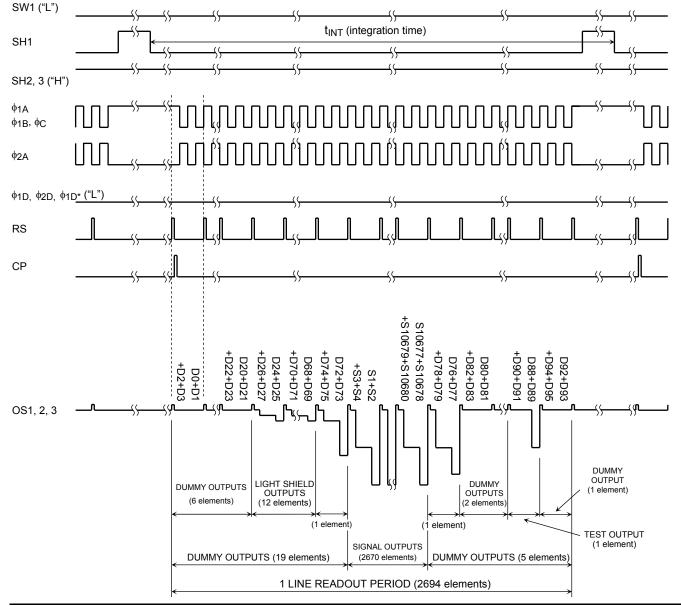
Bearing length 36mm:

The force from upside : 300[N] The force from downside : 200[N] The force from upside : 150[N] The force from downside : 80[N]

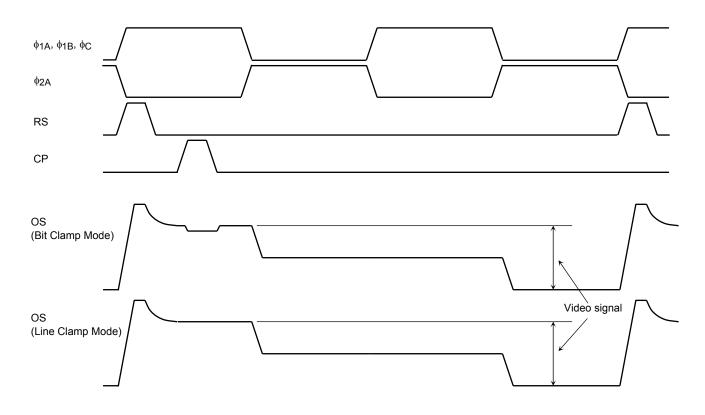
Application Note: Timing Chart (Color 300DPI Mode: Bit Clamp Mode) SW2 = "H"



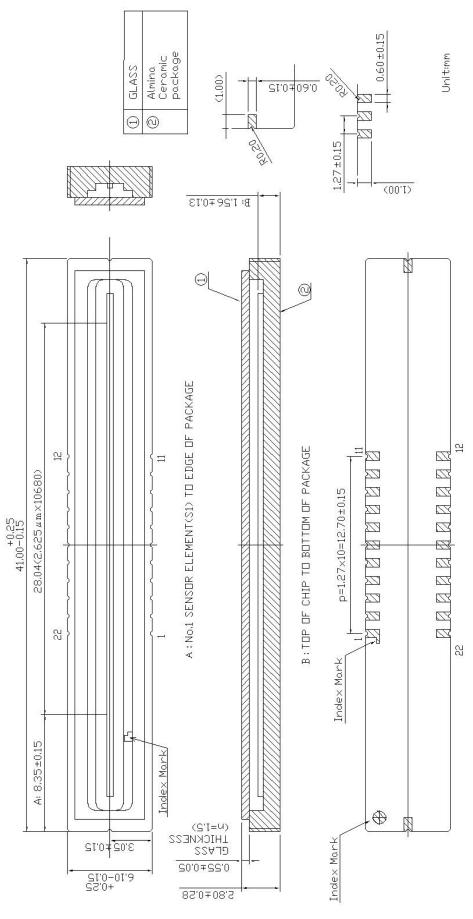
Application Note: Timing Chart (Color 300DPI Mode: Line Clamp Mode) SW2 = "H"



Timing Example (Color 300dpi Mode)



Package Dimensions



Weight: 2.0g (typ.)

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