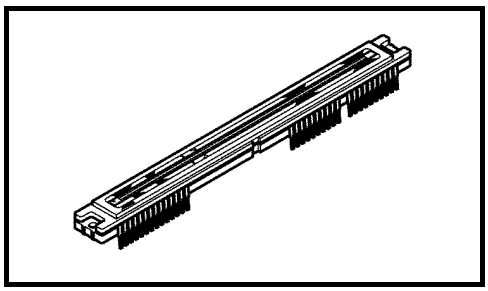
TOSHIBA CCD Linear Image Sensor CCD (Charge Coupled Device)

TENTATIVE

TCD2713DG

The TCD2713DG is a high sensitive and low dark current 7500 pixels × 4 line CCD color image sensor. The sensor is designed for color scanner.

The device contains a row of 7500 pixels × 4 line photodiodes which provide a 24 lines/mm across a A3 size paper.



Weight: 16.0 g (typ.)

Features

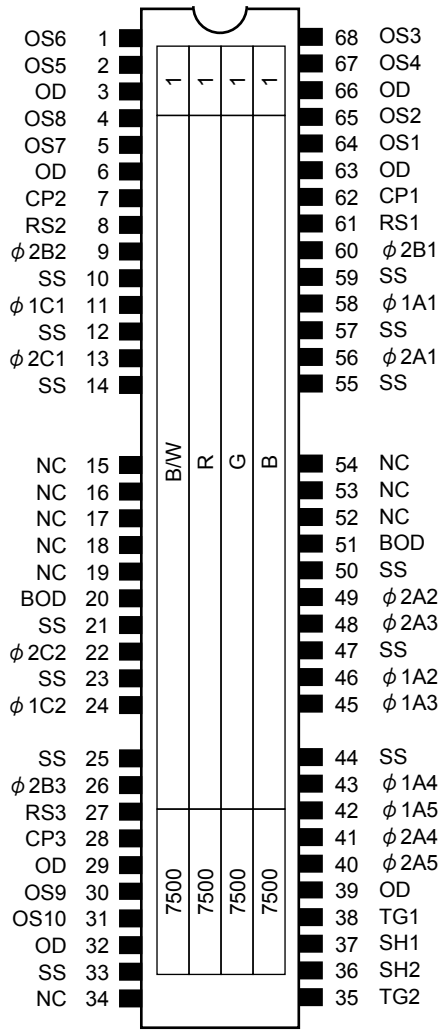
- Number of image sensing pixels : 30000 pixels (7500 pixels × 4 line)
- Image sensing pixels size : 9.325 μm by 9.325 μm on 9.325 μm center
- Photo sensing region : High sensitive pn photodiode
- Clock : 2-phase (5 V)
- Distance between photodiode array
  :Pixel B to pixel G: 18.65 μm (2 lines)
  Pixel G to pixel R: 18.65 μm (2 lines)
  Pixel R to pixel B/W: 55.95 μm (6 lines)
- Internal circuit : Clamp circuit
- Package : 68-pin CERDIP
- Color filter : Red, Green, Blue

Maximum Ratings (Note 1)

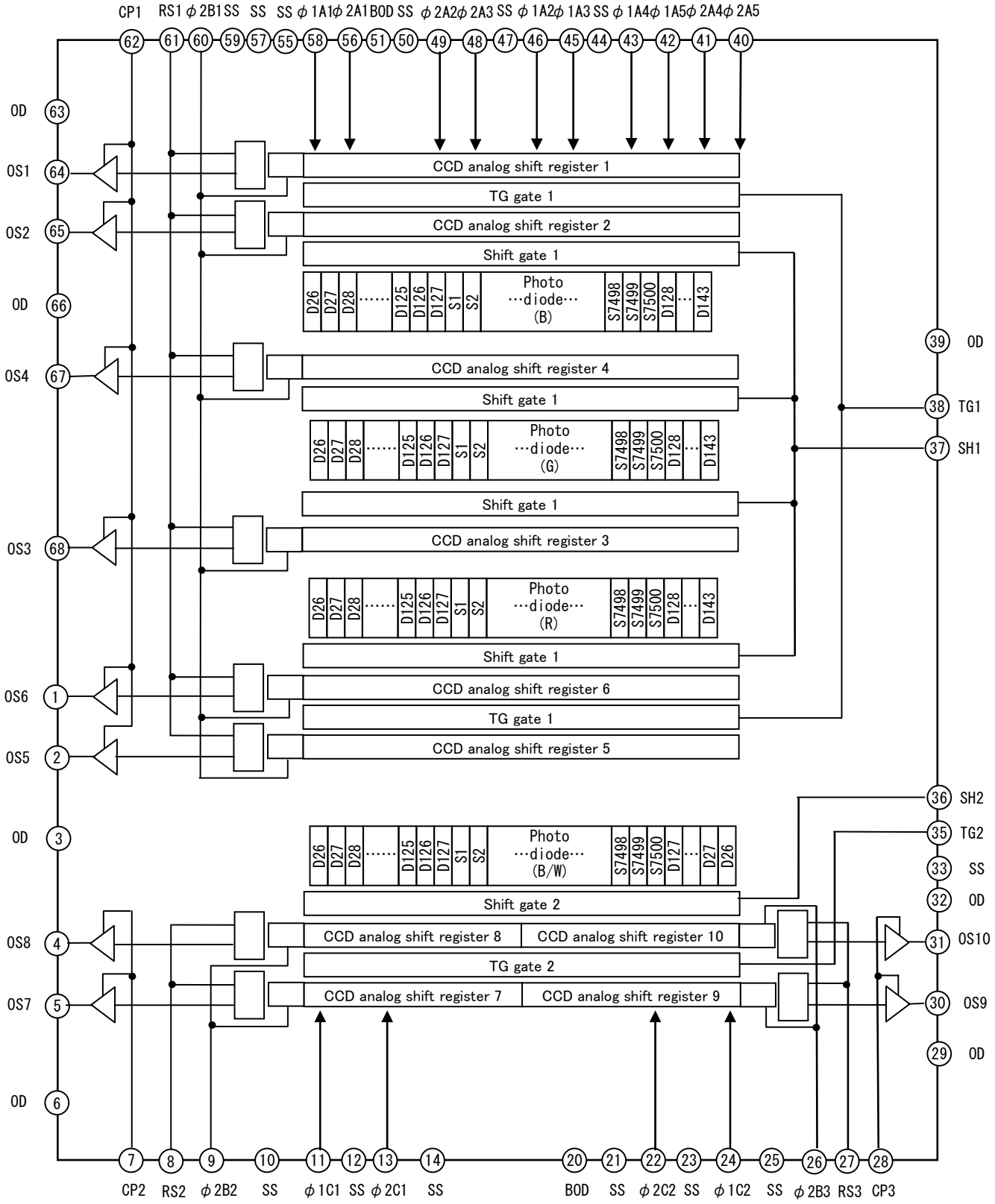
Characteristics	Symbol	Rating	Unit
Clock pulse voltage	$V_{\phi A}$	−0.3~8	V
Clock pulse voltage	$V_{\phi C}$		
Last stage clock pulse voltage	$V_{\phi B}$		
Shift pulse voltage	V_{SH}		
Reset pulse voltage	V_{RS}		
Clamp pulse voltage	V_{CP}		
TG pulse voltage	V_{TG}		
Power supply voltage	V_{OD}	−0.3~13.5	V
Bias power supply voltage	V_{BOD}		
Operating temperature	t_{opr}	0~60	°C
Storage temperature	t_{stg}	−25~85	°C

Note 1: All voltages are with respect to SS pins (ground)

PIN Connections (top view)



Circuit Diagram



Pin Names

Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	OS6	Output signal 6 (RED(EVEN))	35	TG2	TG Gate 2
2	OS5	Output signal 5 (RED(ODD))	36	SH2	Shift gate 2
3	OD	Power supply(RED)	37	SH1	Shift gate 1
4	OS8	Output signal 8 (B/W-F(EVEN))	38	TG1	TG Gate 1
5	OS7	Output signal 7 (B/W-F(ODD))	39	OD	Power supply(COLOR)
6	OD	Power supply(B/W-F)	40	ϕ2A5	Transfer clock (phase 2) COLOR
7	CP2	Clamp gate 2 B/W	41	ϕ2A4	Transfer clock (phase 2) COLOR
8	RS2	Reset gate 2 B/W	42	ϕ1A5	Transfer clock (phase 1) COLOR
9	ϕ2B2	Last stage clock (phase 2) B/W	43	ϕ1A4	Transfer clock (phase 1) COLOR
10	SS	Ground	44	SS	Ground
11	ϕ1C1	Transfer clock (phase 1)B/W	45	ϕ1A3	Transfer clock (phase 1) COLOR
12	SS	Ground	46	ϕ1A2	Transfer clock (phase 1) COLOR
13	ϕ2C1	Transfer clock (phase 2)B/W	47	SS	Ground
14	SS	Ground	48	ϕ2A3	Transfer clock (phase 2) COLOR
15	NC	No connect	49	ϕ2A2	Transfer clock (phase 2) COLOR
16	NC	No connect	50	SS	Ground
17	NC	No connect	51	BOD	Bias power supply
18	NC	No connect	52	NC	No connect
19	NC	No connect	53	NC	No connect
20	BOD	Bias power supply	54	NC	No connect
21	SS	Ground	55	SS	Ground
22	ϕ2C2	Transfer clock (phase 2) B/W	56	ϕ2A1	Transfer clock (phase 2) COLOR
23	SS	Ground	57	SS	Ground
24	ϕ1C2	Transfer clock (phase 1) B/W	58	ϕ1A1	Transfer clock (phase 1) COLOR
25	SS	Ground	59	SS	Ground
26	ϕ2B3	Last stage clock (phase 2) B/W	60	ϕ2B1	Last stage clock (phase 2) COLOR
27	RS3	Reset gate 3 B/W	61	RS1	Reset gate 1 COLOR
28	CP3	Clamp gate 3 B/W	62	CP1	Clamp gate 1 COLOR
29	OD	Power supply(B/W-L)	63	OD	Power supply (BLUE)
30	OS9	Output signal 9 (B/W-L(ODD))	64	OS1	Output signal 1 (BLUE(ODD))
31	OS10	Output signal 10 (B/W-L(EVEN))	65	OS2	Output signal 2 (BLUE(EVEN))
32	OD	Power supply(B/W)	66	OD	Power supply(GREEN)
33	SS	Ground	67	OS4	Output signal 4 (GREEN(EVEN))
34	NC	No connect	68	OS3	Output signal 3 (GREEN(ODD))

Optical/Electrical Characteristics

(Ta = 25°C, V_{OD} = V_{BOD} = 10 V, V_{ϕ} = V_{SH} = V_{RS} = V_{CP}= V_{TG}= 5 V (pulse), f_{ϕ} = 1 MHz, load resistance = 100 kΩ, t_{INT} (integration time) = 10 ms, light source = A light source + CM500S filter (t = 1.0 mm))

●COLOR Part

Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	Red	R (R)	9.2	13.1	17.0	V/lx・s	(Note 2)
	Green	R (G)	12.9	18.4	23.9		
	Blue	R (B)	5.3	7.6	9.8		
Photo response non uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Saturation output voltage		V_{SAT}	1.8	2.0	—	V	(Note 5)
Saturation exposure		SE	0.07	—	—	lx・s	(Note 6)
Dark signal voltage		V_{DRK}	—	3	6	mV	(Note 7)
Dark signal non uniformity		DSNU	—	8	12	mV	(Note 8)
Dc power dissipation		P_D	—	550	770	mW	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z_O	—	0.2	0.5	kΩ	—
Dc signal output voltage		V_{OS}	4.0	5.0	6.0	V	(Note 9)
Random noise		$N_{D\sigma}$	—	1.0	—	mV	(Note 10)

●B/W Part

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	R (B/W)	19.0	23.8	28.5	V/lx・s	(Note 2)
Photo response non uniformity	PRNU (1)	—	10	20	%	(Note 3)
	PRNU (3)	—	3	12	mV	(Note 4)
Saturation output voltage	V_{SAT}	1.8	2.0	—	V	(Note 5)
Saturation exposure	SE	0.06	—	—	lx・s	(Note 6)
Dark signal voltage	V_{DRK}	—	3	6	mV	(Note 7)
Dark signal non uniformity	DSNU	—	8	12	mV	(Note 8)
Dc power dissipation	P_D	—	450	660	mW	—
Total transfer efficiency	TTE	92	98	—	%	—
Output impedance	Z_O	—	0.2	0.5	kΩ	—
Dc signal output voltage	V_{OS}	3.3	4.3	5.3	V	(Note 9)
Random noise	$N_{D\sigma}$	—	0.7	—	mV	(Note 10)

Note 2:Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3:PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{PRNU (1)} = \frac{\Delta\chi}{\bar{\chi}} \times 100 \ (\%)$$

$\bar{\chi}$: Average of total signal outputs
$\Delta\chi$: The maximum deviation from $\bar{\chi}$.

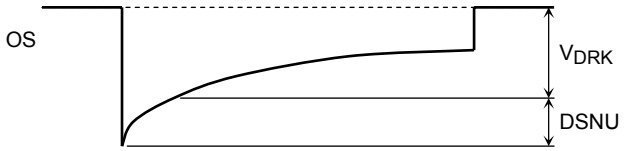
Note 4:PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (typ.).

Note 5:V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

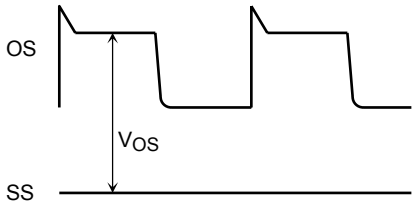
Note 6:Definition of SE: $\text{SE} = \frac{V_{SAT}}{RG}$

Note 7:V_{DRK} is defined as average dark signal voltage of all effective pixels.

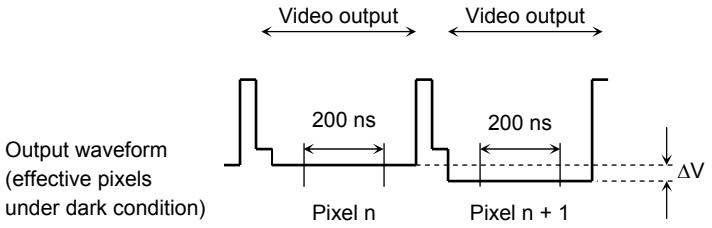
Note 8:DSNU is defined by the difference between average value (V_{DRK}) and the maximum value of the dark voltage.



Note 9:DC signal output voltage is defined as follows:



Note 10:Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark condition) calculated by the following procedure.



1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
2) Each of the output levels at video output periods averaged over 200 nanosecond period to get Vn and Vn + 1.
3) Vn + 1 is subtracted from Vn to get ΔV.
   ΔV = Vn − Vn + 1
4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\Delta V = \frac{1}{30}\sum_{i=1}^{30}|\Delta Vi| \qquad \sigma = \sqrt{\frac{1}{30}\sum_{i=1}^{30}\left(|\Delta Vi| - \overline{\Delta V}\right)^2}$$

5) Procedure 2), 3) and 4) are repeated 10 times to get 10 sigma values.

$$\bar{\sigma} = \frac{1}{10}\sum_{j=1}^{10}\sigma j$$

6) $\bar{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$\text{Random noise} = \frac{1}{\sqrt{2}}\bar{\sigma}$$

Operating Condition (Ta = 25°C)

Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse voltage	"H" level	$V_{\phi 1A}$, $V_{\phi 2A}$	4.75	5	5.5	V
	"L" level	$V_{\phi 1C}$, $V_{\phi 2C}$	0	—	0.25	
Final stage clock pulse voltage	"H" level	$V_{\phi 2B}$	4.75	5	5.5	V
	"L" level		0	—	0.25	
Shift pulse voltage	"H" level	V_{SH}	4.75	5	5.5	V
	"L" level		0	—	0.25	
Reset pulse voltage	"H" level	V_{RS}	4.75	5	5.5	V
	"L" level		0	—	0.25	
Clamp pulse voltage	"H" level	V_{CP}	4.75	5	5.5	V
	"L" level		0	—	0.25	
TG pulse voltage	"H" level	V_{TG}	4.75	5	5.5	V
	"L" level		0	—	0.25	
Power supply voltage		V_{OD}	9.5	10	10.5	
Bias power supply voltage (Note 11)		V_{BOD}	9.5	10	10.5	V

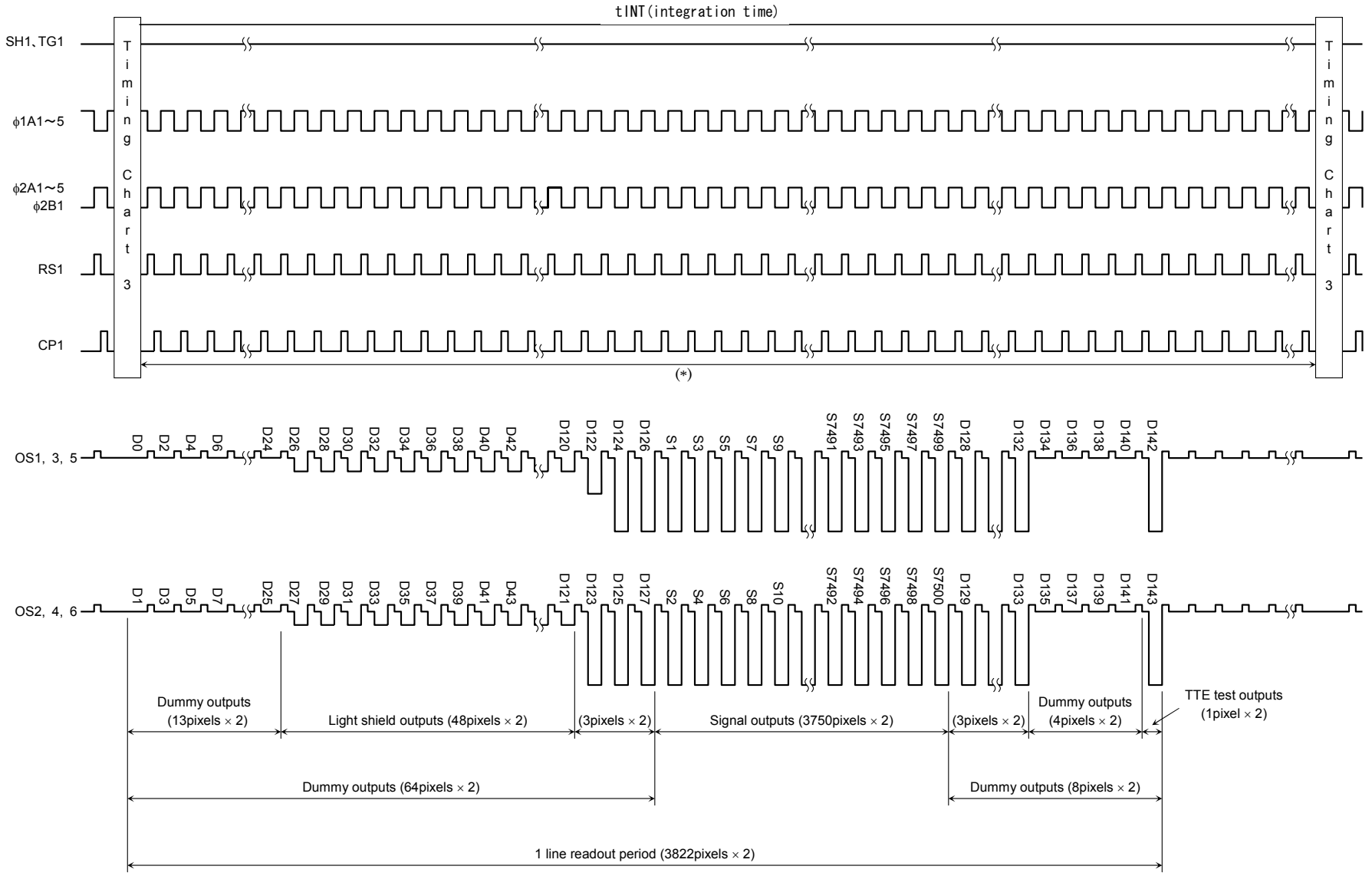
Note 11: Please impress the voltage to V_{BOD} regardless of driving line.

Clock Characteristics (Ta = 25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Clock pulse frequency	f_{ϕ}	—	1	35	MHz
Reset pulse frequency	f_{RS}	—	1	35	MHz
Clamp pulse frequency	f_{CP}	—	1	35	MHz
Clock capacitance (Note 12)	$C_{\phi A}$	—	160	—	pF
	$C_{\phi C}$	—	170	—	pF
Final stage clock capacitance	$C_{\phi B}$	—	10	—	pF
Shift gate capacitance	C_{SH}	—	30	—	pF
Reset gate capacitance	C_{RS}	—	10	—	pF
Clamp gate capacitance	C_{CP}	—	10	—	pF
TG gate capacitance	C_{TG}	—	10	—	pF

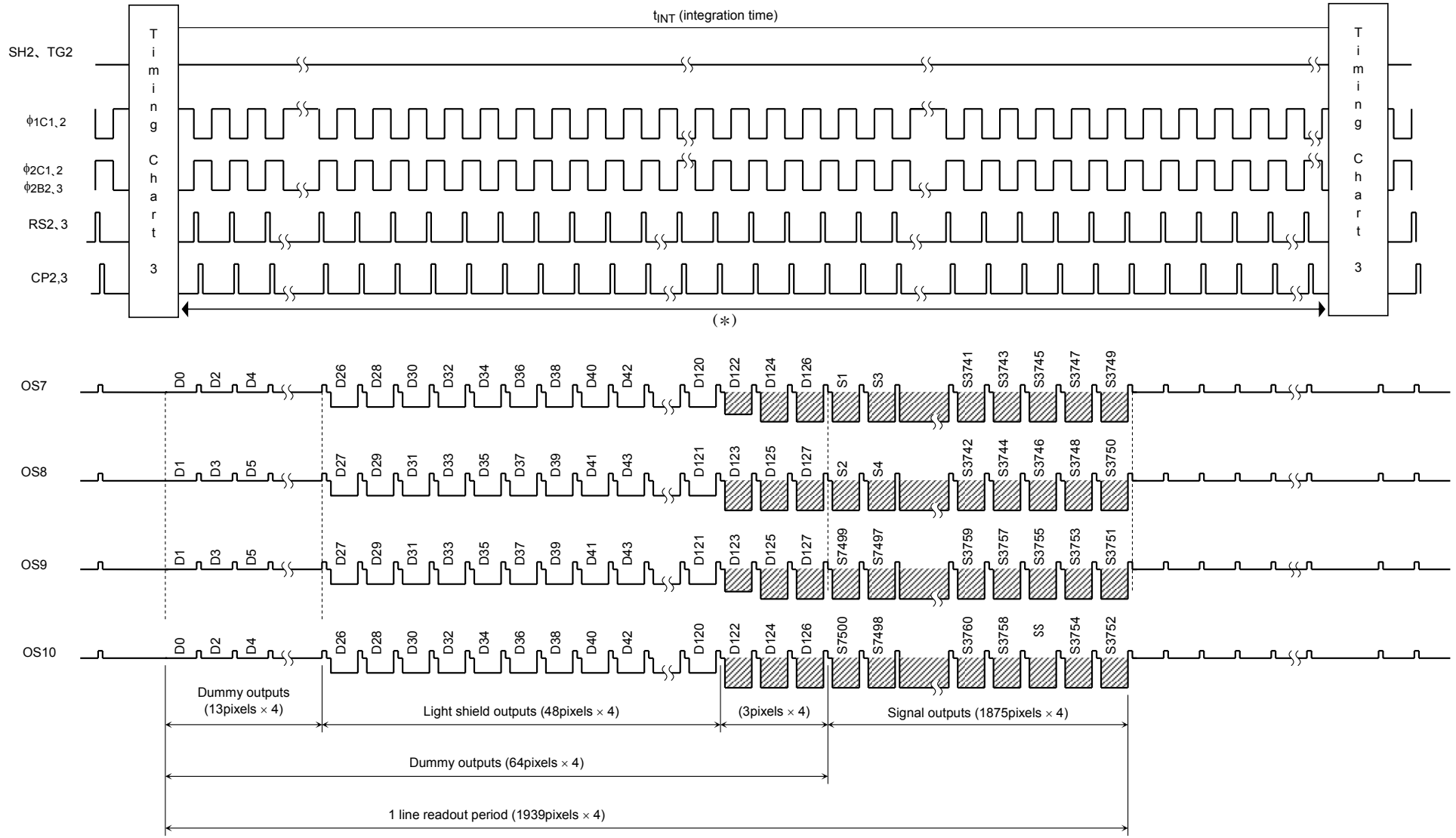
Note 12: $V_{OD} = V_{BOD} = 10$ V

Timing Chart 1: (color part)



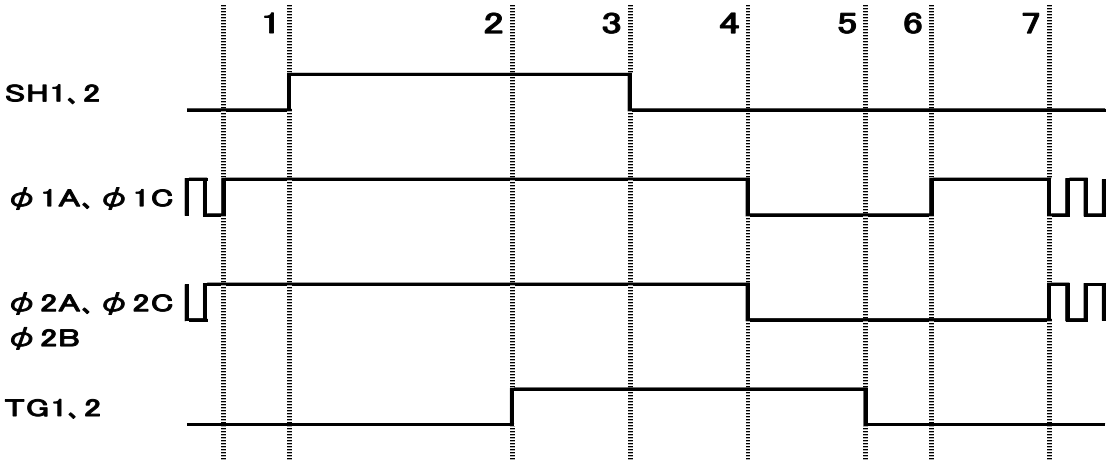
*: Hold the TG1 and SH1 pins at low during this period.

Timing Chart 2 (B/W Part)

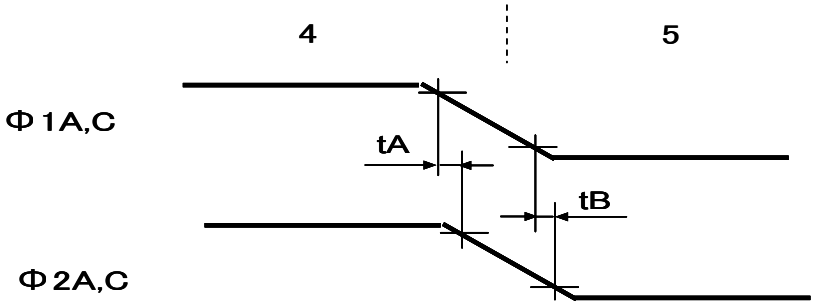


*:Hold the TG2 and SH2 pins at low during this period.

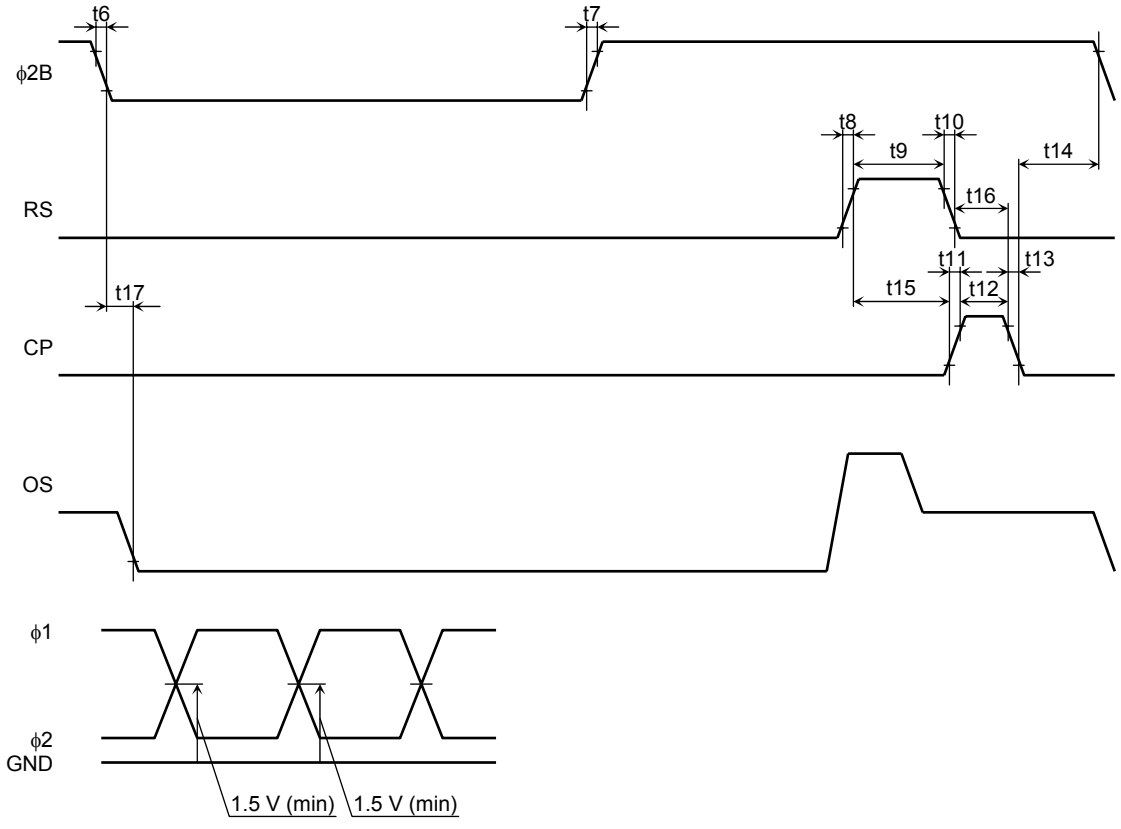
Timing Chart 3



Note13: Each RS and CP pins put to LOW level during the period of the above mentioned address 1-7.



Timing Requirements 1



Characteristics	Symbol	Min	Typ. (Note 14)	Max	Unit
ϕ1, ϕ2 Pulse rise time, fall time	t6, t7	0	50	—	ns
RS pulse rise time, fall time	t8, t10	0	20	—	ns
RS pulse width	t9	6	100	—	ns
CP pulse rise time, fall time	t11, t13	0	20	—	ns
CP pulse width	t12	6	200	—	ns
Pulse timing of ϕ2B and CP	t14	0	40	—	ns
Pulse timing of RS and CP	t15	0	0	—	ns
	t16	6	100	—	ns
Video data delay time (Note 15)	t17	—	7	—	ns

Note14:Measured with fRS=1MHz

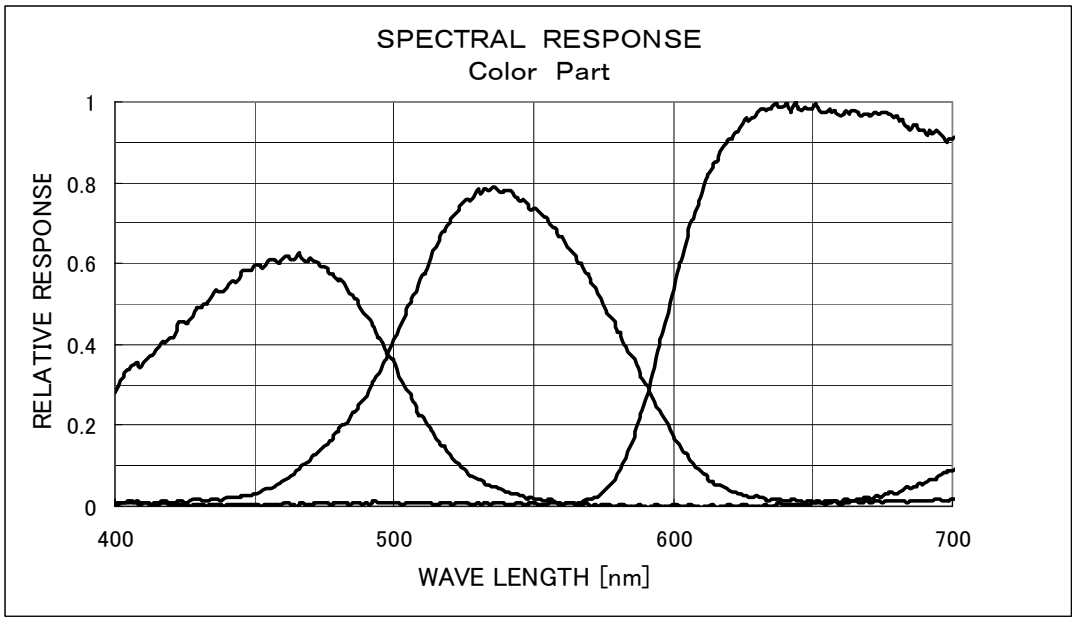
Note15:Load resistance is 100kΩ

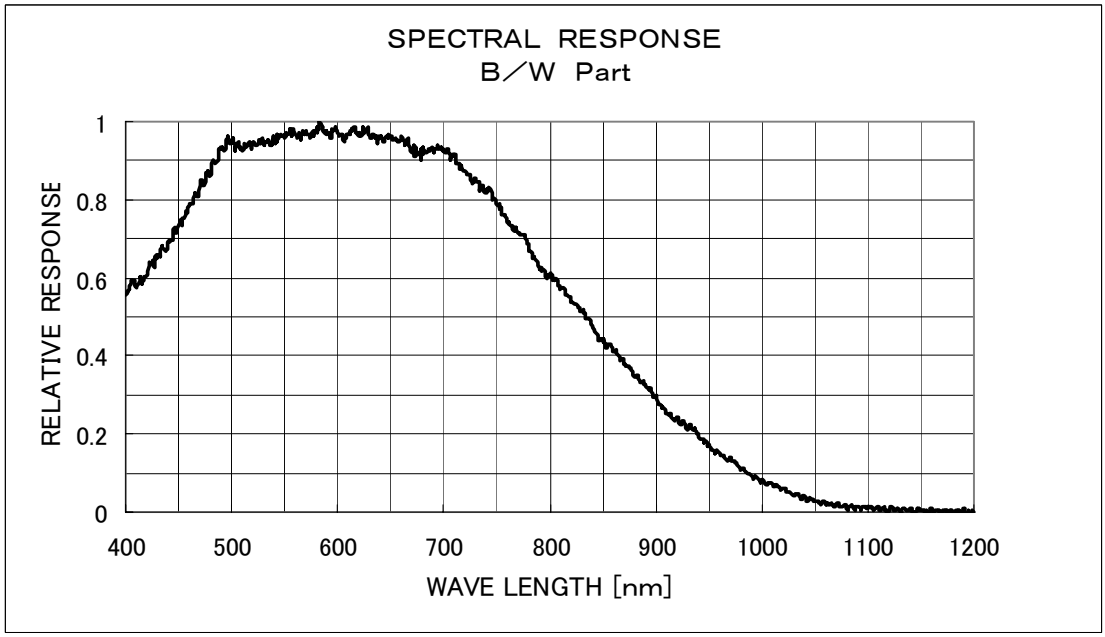
Timing Requirements 2

Timing Address	Min	Typ	Max	Unit
1	250	500	—	ns
2	1000	2000	—	ns
3	500	1000	—	ns
4	500	1000	—	ns
5	500	1000	—	ns
6	250	500	—	ns
7	500	1000	—	ns
Vertical Transfer Time	3.5	7	—	μs

	記号	最小	標準	最大	単位
ϕ1A−ϕ2A(ϕ1C−ϕ2C) Pulse timing	tA	−0.5	0	0.5	ns
	tB	−0.5	0	0.5	ns

Spectral Response





Caution

1. Electrostatic Breakdown

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
Ground the tools such as soldering iron, radio cutting pliers of or pincer.
It is not necessarily required to execute all precaution items for static electricity.
It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

3. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

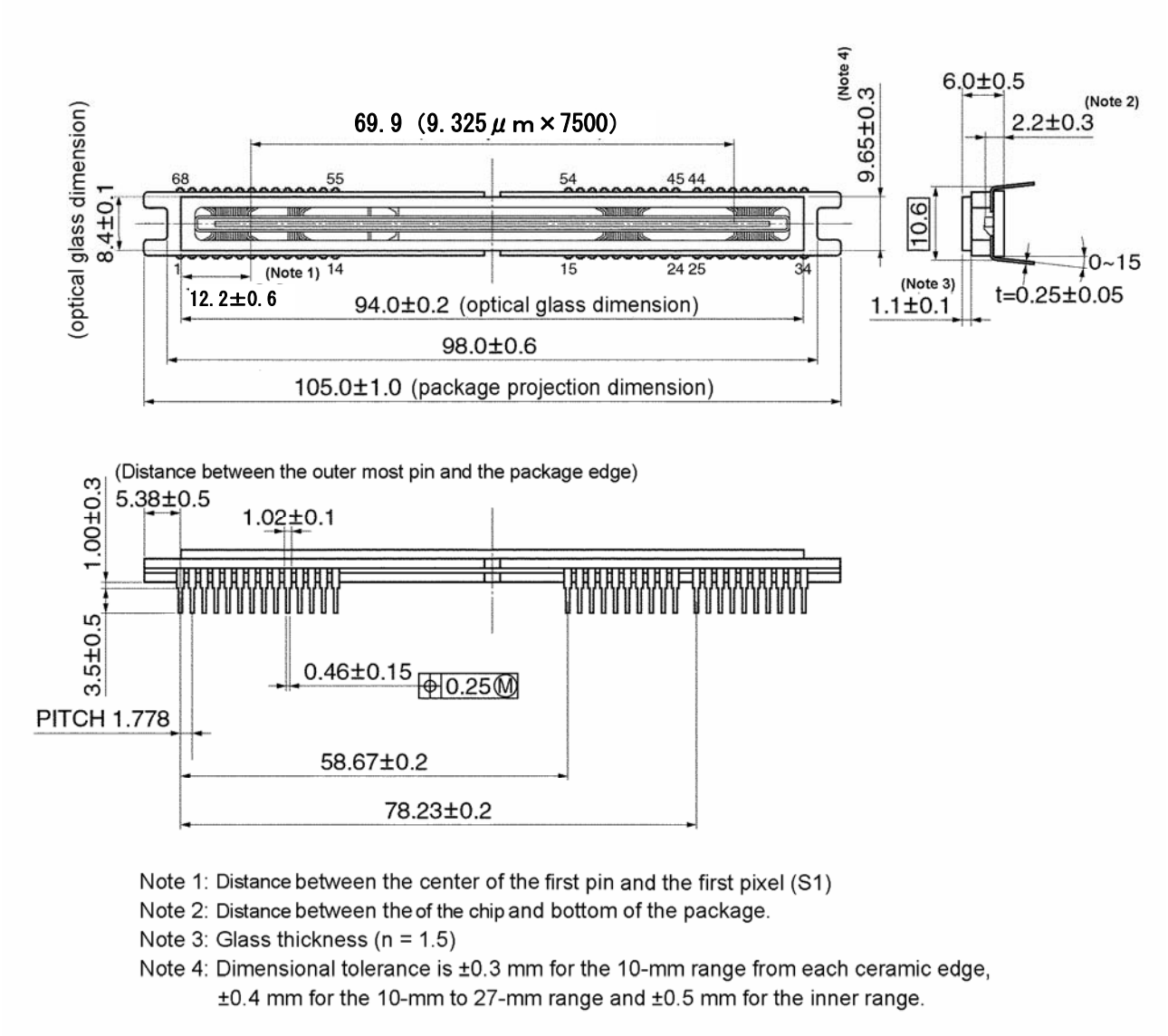
4. Mounting on a PCB

This package is sensitive to mechanical stress.
Toshiba recommends using IC inserters for mounting, instead of using lead forming equipment.

5. Soldering

Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.
Using a soldering iron, complete soldering within three seconds for lead temperatures of up to 380°C.

Package Dimensions



Note 1: Distance between the center of the first pin and the first pixel (S1)
Note 2: Distance between the of the chip and bottom of the package.
Note 3: Glass thickness (n = 1.5)
Note 4: Dimensional tolerance is ±0.3 mm for the 10-mm range from each ceramic edge, ±0.4 mm for the 10-mm to 27-mm range and ±0.5 mm for the inner range.

Weight: 16.0 g (typ.)

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