TOSHIBA CCD Linear Image Sensor CCD (Charge Coupled Device)

TCD1209DG

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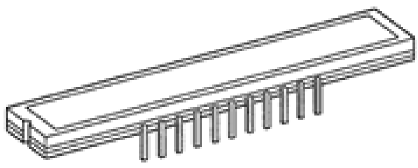
The TCD1209DG is a high sensitive and low dark current 2048 elements CCD linear image sensor.

The device contains a row of 2048 elements photodiodes which provide 8 lines/mm across a B4 size paper. The device is operated by 5.0 V pulse and 12 V power supply.



WDIP22-G-400-2.54H

Features

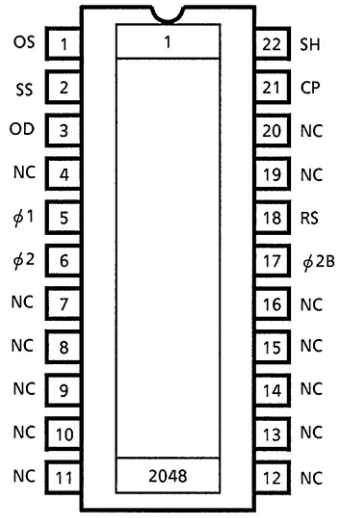
- Number of Image Sensing Elements: 2048 elements
- Image Sensing Element Size: 14μm by 14μm on 14μm center
- Photo Sensing Region: High sensitive PN photodiode
- Clock: 2-phase (5 V)
- Power Supply Voltage: 12 V (typ.)
- Package: 22 pin CERDIP

ABSOLUTE MAXIMUM RATINGS (Note 1)

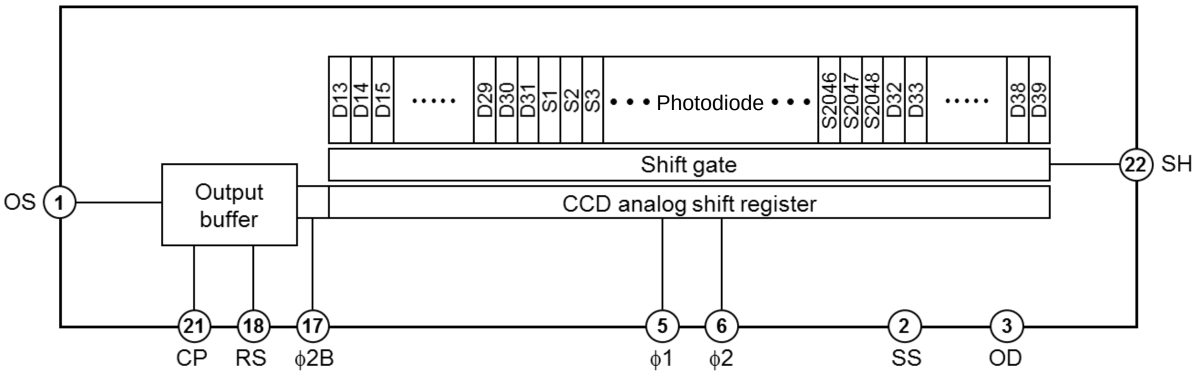
Characteristic	Symbol	Rating	Unit
Clock pulse voltage	V_ϕ	−0.3 to +8.0	V
Shift pulse voltage	V_{SH}		
Reset pulse voltage	V_{RS}		
Clamp pulse voltage	V_{CP}		
Power supply voltage	V_{OD}	-0.3 to +15.0	V
Operating temperature	T_{opr}	−25 to +60	°C
Storage temperature	T_{stg}	−40 to +100	°C

Note 1: All voltages are with respect to SS terminals (ground).
None of the ABSOLUTE MAXIMUM RATINGS must be exceeded, even instantaneously.
If any one of the ABSOLUTE MAXIMUM RATINGS is exceeded, the electrical characteristics, reliability and life time of the device cannot be guaranteed. If the ABSOLUTE MAXIMUM RATINGS are exceeded, the device can be permanently damaged or degraded. Create a system design in such a manner that any of the ABSOLUTE MAXIMUM RATINGS will not be exceeded under any circumstances.

Pin Connections (top view)



Circuit Diagram



Pin Names

Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	OS	Output signal	22	SH	Shift gate
2	SS	Ground	21	CP	Clamp gate
3	OD	Power supply	20	NC	Non connection
4	NC	Non connection	19	NC	Non connection
5	ϕ1	Transfer clock (phase 1)	18	RS	Reset gate
6	ϕ2	Transfer clock (phase 2)	17	ϕ2B	Last stage transfer clock (phase 2)
7	NC	Non connection	16	NC	Non connection
8	NC	Non connection	15	NC	Non connection
9	NC	Non connection	14	NC	Non connection
10	NC	Non connection	13	NC	Non connection
11	NC	Non connection	12	NC	Non connection

Optical/Electrical Characteristics

Ta = 25°C, V_{OD} = 12 V, V_{ϕ} = V_{SH} = V_{RS} = V_{CP} =5 V (pulse), f_{ϕ} = 1.0 MHz, t_{INT} (integration time) = 10 ms, light source = daylight fluorescent lamp

Characteristic	Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	R	25	31	37	V/lx·s	—
Photo response non uniformity	PRNU (1)	—	3	10	%	(Note 2)
	PRNU (3)	—	4	10	mV	(Note 8)
Saturation output voltage	V_{SAT}	1.5	2.0	—	V	(Note 3)
Saturation exposure	SE	0.04	0.06	—	lx·s	(Note 4)
Dark signal voltage	V_{DRK}	—	1.0	2.5	mV	(Note 5)
Dark signal non uniformity	DSNU	—	1.0	2.5	mV	(Note 5)
DC power dissipation	P_D	—	160	400	mW	—
Total transfer efficiency	TTE	92	98	—	%	—
Output impedance	Z_O	—	0.2	1.0	kΩ	—
Dynamic range	DR	—	2000	—	—	(Note 6)
DC output signal voltage	V_{OS}	4.0	5.5	7.0	V	(Note 7)
Random noise	$N_{D\sigma}$	—	0.6	—	mV	(Note 9)

Note 2: PRNU (1) is defined on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature, where measured approximately 500 mV of signal output.

$$\mathrm{PRNU}(1) = \frac{\Delta X}{\overline{X}} \times 100\ (\%)$$

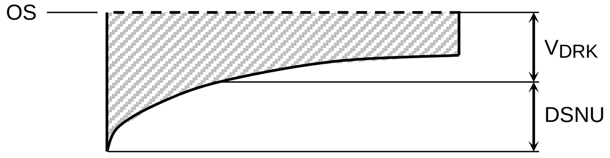
$\overline{X}$: Average of total signal outputs
ΔX: The maximum deviation from $\overline{X}$

Note 3: V_{SAT} is defined as the minimum saturation output voltage of all effective pixels.

Note 4: Definition of SE:

$$SE = \frac{V_{SAT}}{R}$$

Note 5: V_{DRK} is defined as average dark signal voltage of all effective pixels.
DSNU is defined by the difference between average value (V_{DRK}) and the maximum value of the dark voltage.

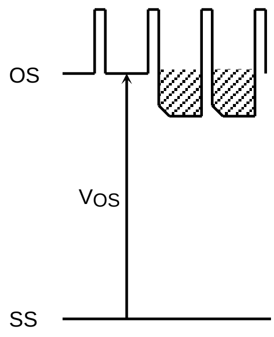


Note 6: Definition of DR:

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

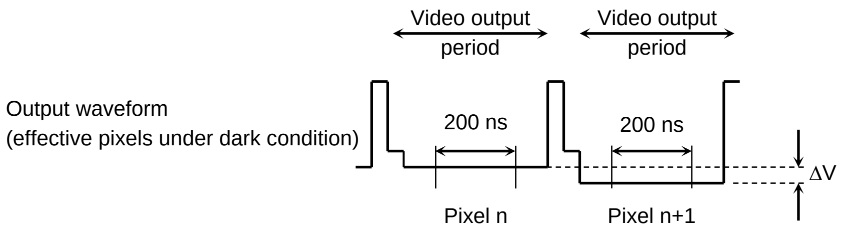
V_{DRK} is proportional to t_{INT} (integration time). So the shorter integration time makes wider dynamic range.

Note 7: DC output signal voltage is defined as follows.



Note 8: PRNU (3) is defined as the maximum voltage with next pixel, where measured approximately 50 mV of signal output.

Note 9: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark condition) calculated by the following procedure.



1) Two adjacent pixels (pixel n and n+1) in one reading are fixed as measurement points.
2) Each of the output levels at video output periods averaged over 200 ns period to get V(n) and V(n+1).
3) V(n+1) is subtracted from V(n) to get ΔV.

$$\Delta V = V(n) - V(n+1)$$

4) The standard deviation of ΔV is calculated after procedure 2) and 3) are repeated 30 times (30 readings).

$$\overline{\Delta V} = \frac{1}{30}\sum_{i=1}^{30}\left|\Delta V i\right| \qquad \sigma = \sqrt{\frac{1}{30}\sum_{i=1}^{30}\left(\left|\Delta V i\right| - \overline{\Delta V}\right)^2}$$

5) Procedure 2), 3) and 4) are repeated 10 times to get sigma value.
6) 10 sigma values are averaged.

$$\bar{\sigma} = \frac{1}{10}\sum_{j=1}^{10}\sigma j$$

7) $\bar{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$ND\sigma = \frac{1}{\sqrt{2}}\bar{\sigma}$$

Recommended Operating Conditions (Ta = 25°C)

For best performance, the device should be used within the Recommended Operating Conditions.

Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse voltage	“H” level	$V_{\phi1}$ $V_{\phi2}$	4.5	5.0	5.5	V
	“L” level		0	0	0.5	
Last stage clock pulse voltage	“H” level	$V_{\phi2B}$	4.5	5.0	5.5	V
	“L” level		0	0	0.5	
Shift pulse voltage	“H” level	V_{SH}	4.5	5.0	5.5	V
	“L” level		0	0	0.5	
Reset pulse voltage	“H” level	V_{RS}	4.5	5.0	5.5	V
	“L” level		0	0	0.5	
Clamp pulse voltage	“H” level	V_{CP}	4.5	5.0	5.5	V
	“L” level		0	0	0.5	
Power supply voltage		V_{OD}	11.4	12.0	13.0	V

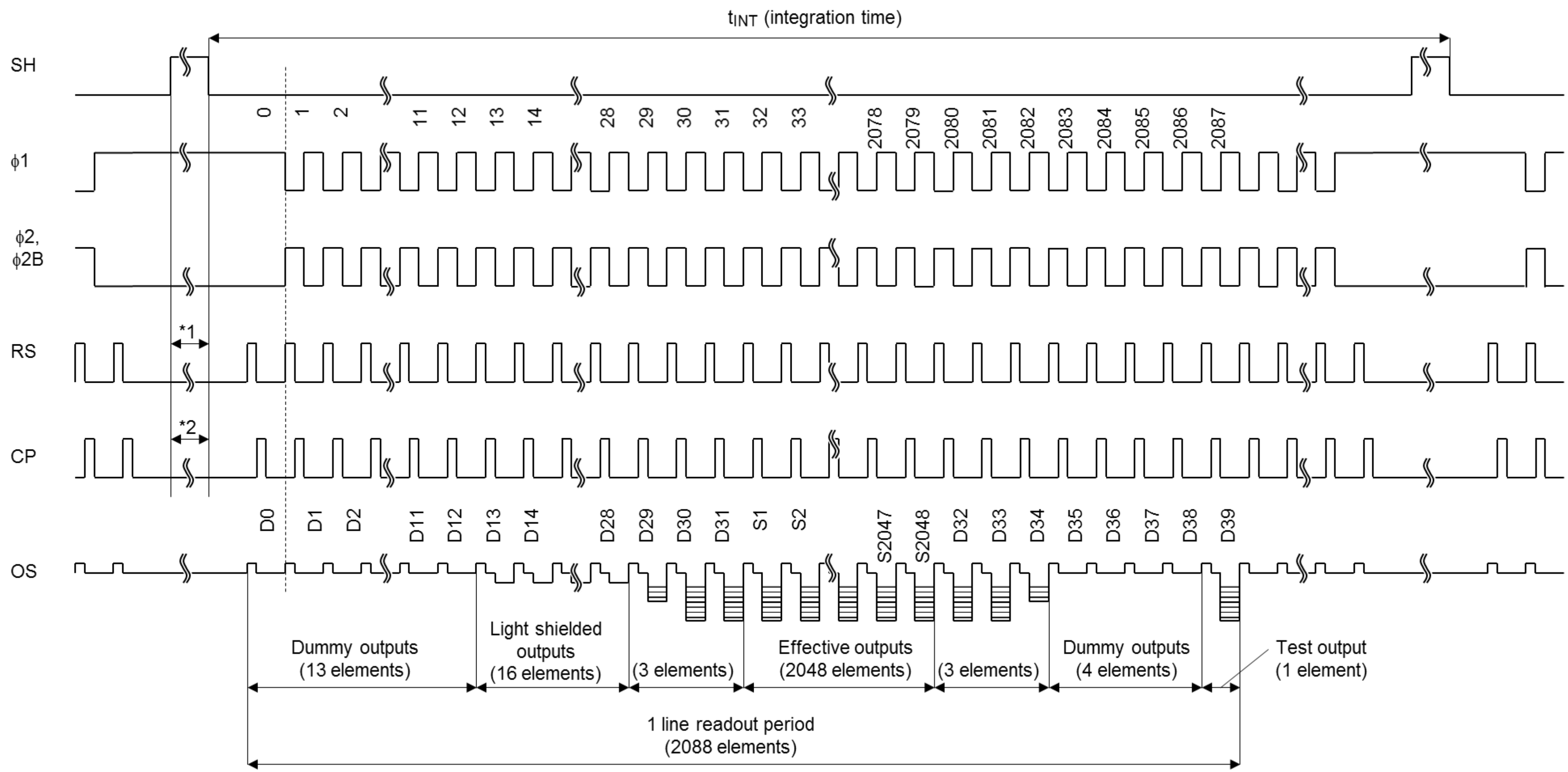
Clock Characteristics (Ta = 25°C)

For best performance, the device should be used within the Recommended Operating Conditions.

Characteristic	Symbol	Min	Typ.	Max	Unit
Clock pulse frequency	f_{ϕ}	—	1	20	MHz
Reset pulse frequency	f_{RS}	—	1	20	MHz
Clock capacitance (Note 10)	$C_{\phi1}$	—	200	—	pF
	$C_{\phi2}$	—	200	—	pF
Last stage clock capacitance	$C_{\phi2B}$	—	10	20	pF
Shift gate capacitance	C_{SH}	—	30	—	pF
Reset gate capacitance	CRS	—	10	20	pF
Clamp gate capacitance	C_{CP}	—	10	20	pF

Note 10: V_{OD} = 12 V

Timing Chart

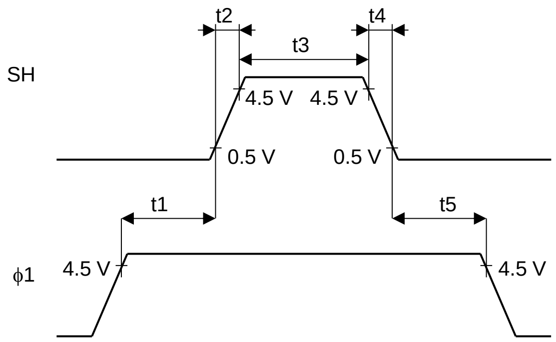


*1: Keep the RS pin "L" level.

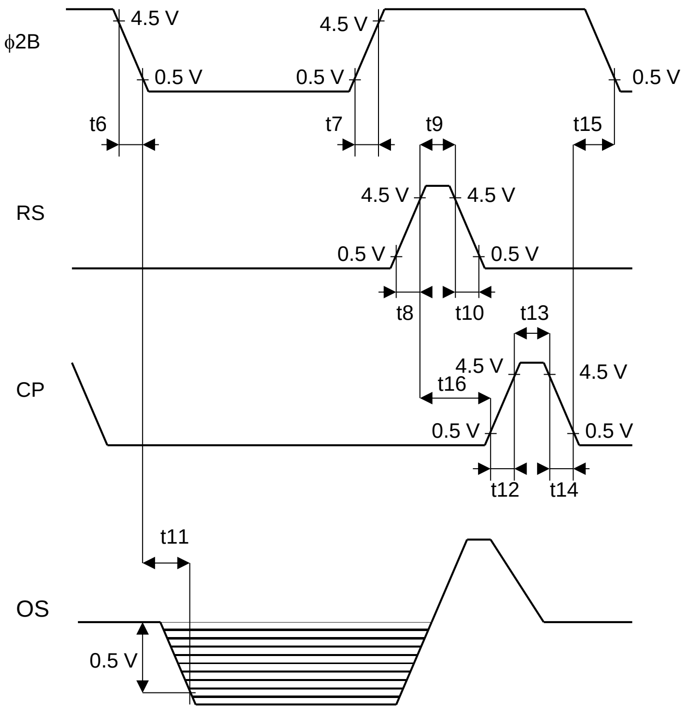
*2: Keep the CP pin "L" level.

Timing Requirements

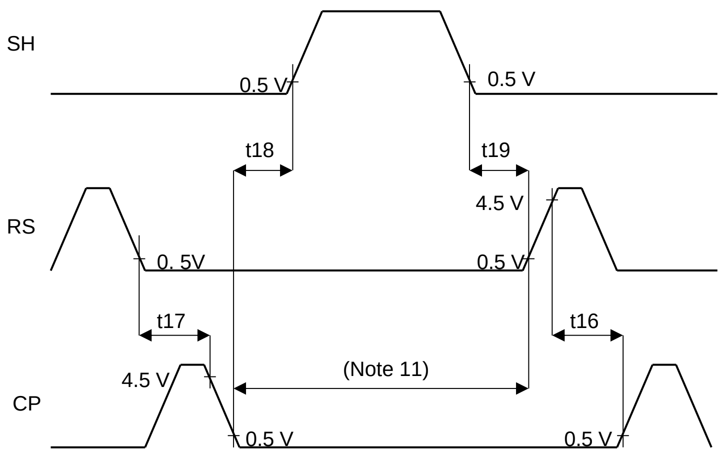
SH,ϕ1 Timing



ϕ2B, RS, CP Timing

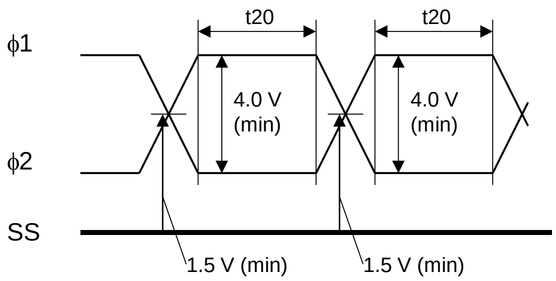


SH,RS,CP Timing



Note 11: Keep the RS and CP pins “L” level.

ϕ1, ϕ2 Cross point



Characteristic	Symbol	Min	Typ. (Note 12)	Max	Unit
Pulse timing of SH and ϕ1	t1, t5	200 +t8+t12+t13+t14 +t16	500	—	ns
SH pulse rise time, fall time	t2, t4	0	50	—	ns
SH pulse width	t3	1000	1500	—	ns
ϕ2B pulse rise time, fall time	t6, t7	0	100	—	ns
RS pulse rise time, fall time	t8, t10	0	20	—	ns
RS pulse width	t9	10	100	—	ns
Video data delay time	t11	—	15	—	ns
CP pulse rise time, fall time	t12, t14	0	20	—	ns
CP pulse width	t13	10	100	—	ns
Pulse timing of ϕ2B and CP	t15	0	50	—	ns
Pulse timing of RS and CP	t16	0	100	—	ns
	t17	10	100	—	ns
Pulse timing of SH and CP	t18	200	—	—	ns
Pulse timing of SH and RS	t19	200	—	—	ns
Pulse timing of ϕ1 and ϕ2	t20	17	—	—	ns

Note 12: Measured with $f_{\phi} = 1$ MHz.

Cautions

1. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.
CCD Image Sensor is protected against static electricity, but inferior puncture mode device due to static electricity is sometimes detected. In handing the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
c. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
d. Ionized air is recommended for discharge when handling CCD image sensors.

It is not necessarily required to execute all precaution items for static electricity.
It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N_2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

3. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Mounting on a PCB

This package is sensitive to mechanical stress.
TOSHIBA recommends using IC inserters for mounting, instead of using lead forming equipment.
Since this package is not strong against mechanical stress, you should not reform the lead frame.
We recommend to use an IC-inserter when you assemble to PCB.

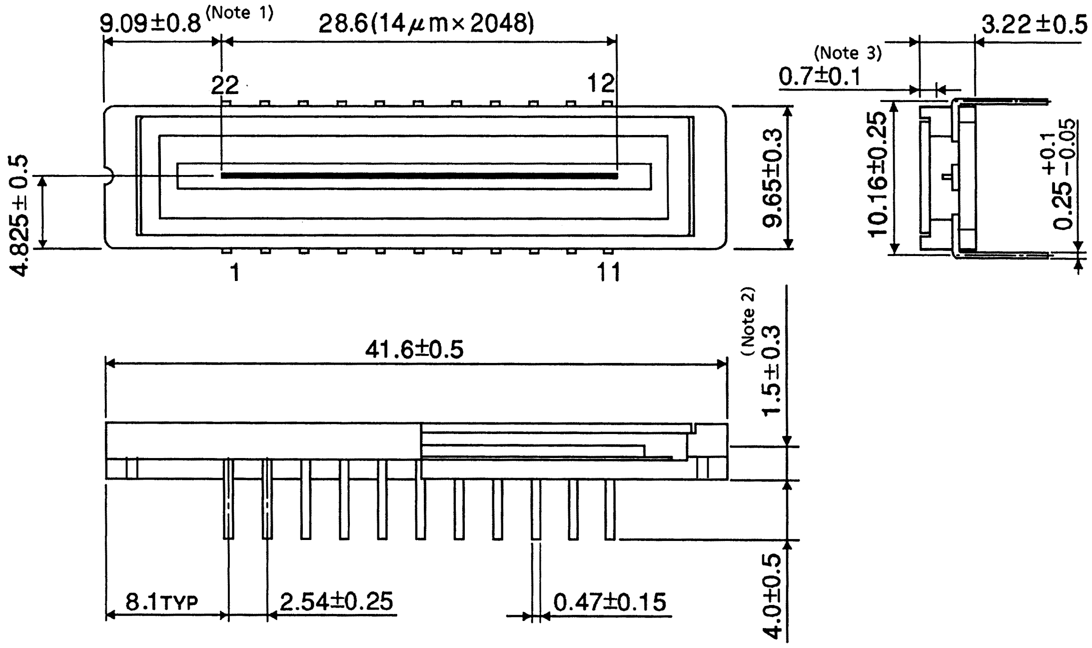
5. Soldering

Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.
Using a soldering iron, complete soldering within three seconds for lead temperatures of up to 350°C.

Package Dimensions

WDIP22-G-400-2.54H

Unit: mm



Note 1: Distance between the edge of the package and the first pixel (S1)
Note 2: Distance between the top of chip and bottom of the package
Note 3: Glass thickness (n = 1.5)

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