

[Product Information]

IMX367LLA

Ver.1.1

Diagonal 21.6 mm (Type 4 / 3) CMOS solid-state Image Sensor with Square Pixel for Monochrome Cameras

Description

The IMX367LLA is a diagonal 21.6 mm (Type 4 / 3) CMOS active pixel type solid-state image sensor with a square pixel array and 19.66 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and low PLS characteristics are achieved.

(Applications: FA cameras, ITS cameras)

Features

- ◆ CMOS active pixel type dots
- ◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆ Global shutter function
- ◆ Input frequency
37.125 MHz / 74.25 MHz / 54 MHz
- ◆ Number of recommended recording pixels: 4416 (H) × 4428 (V) approx. 19.55 M pixels
 - Readout mode
 - All-pixel scan mode
 - Vertical / Horizontal 1 / 2 Subsampling mode
 - 2 × 2 Vertical FD binning mode
 - ROI mode
 - Vertical / Horizontal - Normal / Inverted readout mode
- ◆ Readout rate
 - Maximum frame rate in
 - All-pixel scan mode: 8 bit: 43.0 frame/s, 10 bit: 39.6 frame/s, 12 bit: 28.3 frame/s
- ◆ 8-bit / 10-bit / 12-bit A/D converter
- ◆ CDS / PGA function
 - 0 dB to 24 dB: Analog Gain (0.1 dB step)
 - 24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- ◆ I/O interface
 - SLVS (2 ch / 4 ch / 8 ch switching) output (594 / 297 Mbps per ch)
 - SLVS - EC (1 Lane / 2 Lane / 4 Lane / 8 Lane) output (2.376 / 1.188 Gbps per Lane)
- ◆ Recommended lens F number: 2.8 or more (Close side)
- ◆ Recommended exit pupil distance: -100 mm to $-\infty$

Pregius

* Pregius is a trademark of Sony Corporation. The Pregius is global shutter pixel technology for active pixel-type CMOS image sensors that use Sony's low-noise CCD structure, and realizes high picture quality.

Sony reserves the right to change products and specifications without prior notice.

Sony logo is a registered trademark of Sony Corporation.

Device Structure

◆ CMOS image sensor			
◆ Image size	Diagonal 21.6 mm (Type 4 / 3)	Approx. 19.66 M pixels	All-pixel
◆ Total number of pixels	4432 (H) × 4446 (V)	Approx. 19.70 M pixels	
◆ Number of effective pixels	4432 (H) × 4436 (V)	Approx. 19.66 M pixels	
◆ Number of active pixels	4432 (H) × 4436 (V)	Approx. 19.66 M pixels	
◆ Number of recommended recording pixels	4416 (H) × 4428 (V)	Approx. 19.55 M pixels	All-pixel
◆ Unit cell size	3.45 μm (H) × 3.45 μm (V)		
◆ Optical black	Horizontal (H) direction: Front 0 pixel, rear 0 pixel Vertical (V) direction: Front 10 pixels, rear 0 pixel		
◆ Package	236 pin PGA		

Image Sensor Characteristics (Preliminary)

(Tj = 60 °C)

Item		Value	Remarks
Sensitivity (F8)	Typ.	915 mV	1/30 s accumulation
Saturation signal	Min.	1001 mV	

Basic Drive Mode

Drive mode	Recommended number of recording pixels	Maximum frame rate [frame/s]	Output interface	ADC [bit]
All pixel	4416 (H) × 4428 (V) approx. 19.55 M pixels	28.0	SLVS 8 ch	8
		43.0	SLVS – EC 8 Lane	
		22.7	SLVS 8 ch	10
		39.6	SLVS – EC 8 Lane	
		19.0	SLVS 8 ch	12
		28.3	SLVS – EC 8 Lane	
Vertical / Horizontal 1/2 subsampling	2208 (H) × 2214 (V) approx. 4.89 M pixels	84.2	SLVS 8 ch	8
		84.2	SLVS – EC 8 Lane	
		77.7	SLVS 8 ch	10
		77.7	SLVS – EC 8 Lane	
		55.7	SLVS 8 ch	12
		55.7	SLVS – EC 8 Lane	
2 × 2 Vertical FD binning mode	2208 (H) × 2214 (V) approx. 4.89 M pixels	84.2	SLVS 8 ch	8
		84.2	SLVS – EC 8 Lane	
		77.7	SLVS 8 ch	10
		77.7	SLVS – EC 8 Lane	
		55.7	SLVS 8 ch	12
		55.7	SLVS – EC 8 Lane	

[Product Information]

IMX367LQA

Ver.1.0

Diagonal 21.6 mm (Type 4 / 3) CMOS solid-state Image Sensor with Square Pixel for Color Cameras

Description

The IMX367LQA is a diagonal 21.6 mm (Type 4 / 3) CMOS active pixel type solid-state image sensor with a square pixel array and 19.66 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and low PLS characteristics are achieved.
(Applications: FA cameras, ITS cameras)

Features

- ◆ CMOS active pixel type dots
- ◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆ Global shutter function
- ◆ Input frequency
37.125 MHz / 74.25 MHz / 54 MHz
- ◆ Number of recommended recording pixels: 4416 (H) × 4428 (V) approx. 19.55 M pixels
 - Readout mode
 - All-pixel scan mode
 - Vertical / Horizontal 1 / 2 Subsampling mode
 - ROI mode
 - Vertical / Horizontal - Normal / Inverted readout mode
- ◆ Readout rate
 - Maximum frame rate in
 - All-pixel scan mode: 8 bit: 43.0 frame/s, 10 bit: 39.6 frame/s, 12 bit: 28.3 frame/s
- ◆ 8-bit / 10-bit / 12-bit A/D converter
- ◆ CDS / PGA function
 - 0 dB to 24 dB: Analog Gain (0.1 dB step)
 - 24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- ◆ I/O interface
 - SLVS (2 ch / 4 ch / 8 ch switching) output (594 / 297 Mbps per ch)
 - SLVS - EC (1 Lane / 2 Lane / 4 Lane / 8 Lane) output (2.376 / 1.188 Gbps per Lane)
- ◆ Recommended lens F number: 2.8 or more (Close side)
- ◆ Recommended exit pupil distance: -100 mm to $-\infty$

Pregius

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Device Structure

◆ CMOS image sensor			
◆ Image size	Diagonal 21.6 mm (Type 4 / 3)	Approx. 19.66 M pixels	All-pixel
◆ Total number of pixels	4432 (H) × 4446 (V)	Approx. 19.70 M pixels	
◆ Number of effective pixels	4432 (H) × 4436 (V)	Approx. 19.66 M pixels	
◆ Number of active pixels	4432 (H) × 4436 (V)	Approx. 19.66 M pixels	
◆ Number of recommended recording pixels	4416 (H) × 4428 (V)	Approx. 19.55 M pixels	All-pixel
◆ Unit cell size	3.45 μm (H) × 3.45 μm (V)		
◆ Optical black	Horizontal (H) direction: Front 0 pixel, rear 0 pixel Vertical (V) direction: Front 10 pixels, rear 0 pixel		
◆ Package	236 pin PGA		

Image Sensor Characteristics (Preliminary)

(Tj = 60 °C)

Item		Value	Remarks
Sensitivity (F5.6)	Typ.	1146 mV	1/30 s accumulation
Saturation signal	Min.	1001 mV	

Basic Drive Mode

Drive mode	Recommended number of recording pixels	Maximum frame rate [frame/s]	Output interface	ADC [bit]
All pixel	4416 (H) × 4428 (V) approx. 19.55 M pixels	28.0	SLVS 8 ch	8
		43.0	SLVS – EC 8 Lane	
		22.7	SLVS 8 ch	10
		39.6	SLVS – EC 8 Lane	
		19.0	SLVS 8 ch	12
		28.3	SLVS – EC 8 Lane	
Vertical / Horizontal 1/2 subsampling	2208 (H) × 2214 (V) approx. 4.89 M pixels	84.2	SLVS 8 ch	8
		84.2	SLVS – EC 8 Lane	
		77.7	SLVS 8 ch	10
		77.7	SLVS – EC 8 Lane	
		55.7	SLVS 8 ch	12
		55.7	SLVS – EC 8 Lane	