Preliminary

C650

256X512 ELEMENTS AREA ARRAY

IMAGE SENSOR

DATA SHEET

1. GENERAL DESCRIPTION

The C650, 256x512 elements area array active pixel sensor is designed to provide a large pixel size, slow scan, low power consumption for space and machine vision applications. The C650 is mixed mode silicon on chip (SOC) IC. It combines analog circuitry, digital circuitry and optical sensor circuitry into a tiny chip. This chip integrates a 256x512 active pixel sensor array, a PGA for row wise gain compensation, I^2C interface, SRAM, 12 bit analog to digital (ADC), voltage regulator, low voltage differential amplifier (LVDS) and timing generator together. The device can be operated in imaging mode or power down mode. Device settings, including coarse gain, row wise PGA gain, ADC input selection, data output type selection and operating modes can be readable through the I^2C interface. Furthermore, the row wise PGA gain can be setting with this interface and the coarse gain can be latched through external latch start pulse.

This device used CMOS Sensor's proprietary advanced APS technology and readout structure to reduce the fixed pattern noise, increase dynamic range and improve linearity. The pixel size is 50 um square on an element pitch of 50 um. The device cans response over the spectral wavelength of 400 to 950 nm.

2. FEATURES

- 50 um x 50 um pixel size
- 50 um element pitch
- 256x512 active elements; In addition, 20, 10 dummy elements on left, right side for each row and 2 rows of dummy elements at top, bottom side respectively
- 25600 um x 12800 um image size
- Single video readout, 12 bit resolution, selectable serial/parallel readout mode
- Support two different readout modes: imaging readout and power down
- Start and stop integration for all pixels simultaneously (snap shot operation)
- Auto dark voltage cancellation and fixed pattern noise cancellation
- Programmable gain control feature: one bit for coarse gain of (x1 and x2) and seven bits for row wise gain compensation
- I^2C interface feature: row wise PGA gain controllable externally; Device setting status readable
- Global exposure control function. No integration will take place till exposure control is active
- ADC input selection to select either internal PGA output or external input voltage to be connected to ADC input

- Independent pins to set the device for gain, ADC input selection, dark voltage cancellation selection, output data type and power down mode. All input setting pin is provided in CMOS interface. The gain setting pin is latched by an external latch start pulse (LSP)

3. APPLICATIONS

- Machine Vision, Auto Vision Inspection

4. DEVICE DESCRIPTION

4.1 System Overview

Figure 1 shows a functional block diagram of the C650 active pixel sensor. It includes the following functions.

- 256x512 active pixels and total number of pixels including dummy pixel is 286x516
- Fixed pattern suppression circuitry
- Dark voltage cancellation circuitry
- Programmable gain amplifier (PGA) for gain control
- Row wise gain alteration for spectral response compensation by PGA gain variation
- 12 bit analog to digital converter (ADC)
- Global exposure control circuitry
- Timing generator to generate internal clock with approximate timing
- Power down mode through external command
- Low voltage differential signal driver / receiver for clocks and data line
- Data format for ADC data output serialization
- Band gap and voltage regulator for referencing ADC and PGA
- Inter connect I^2C interface for commanding and reading the device settings
- Divided by 12 counter for internal timing generator from external clock

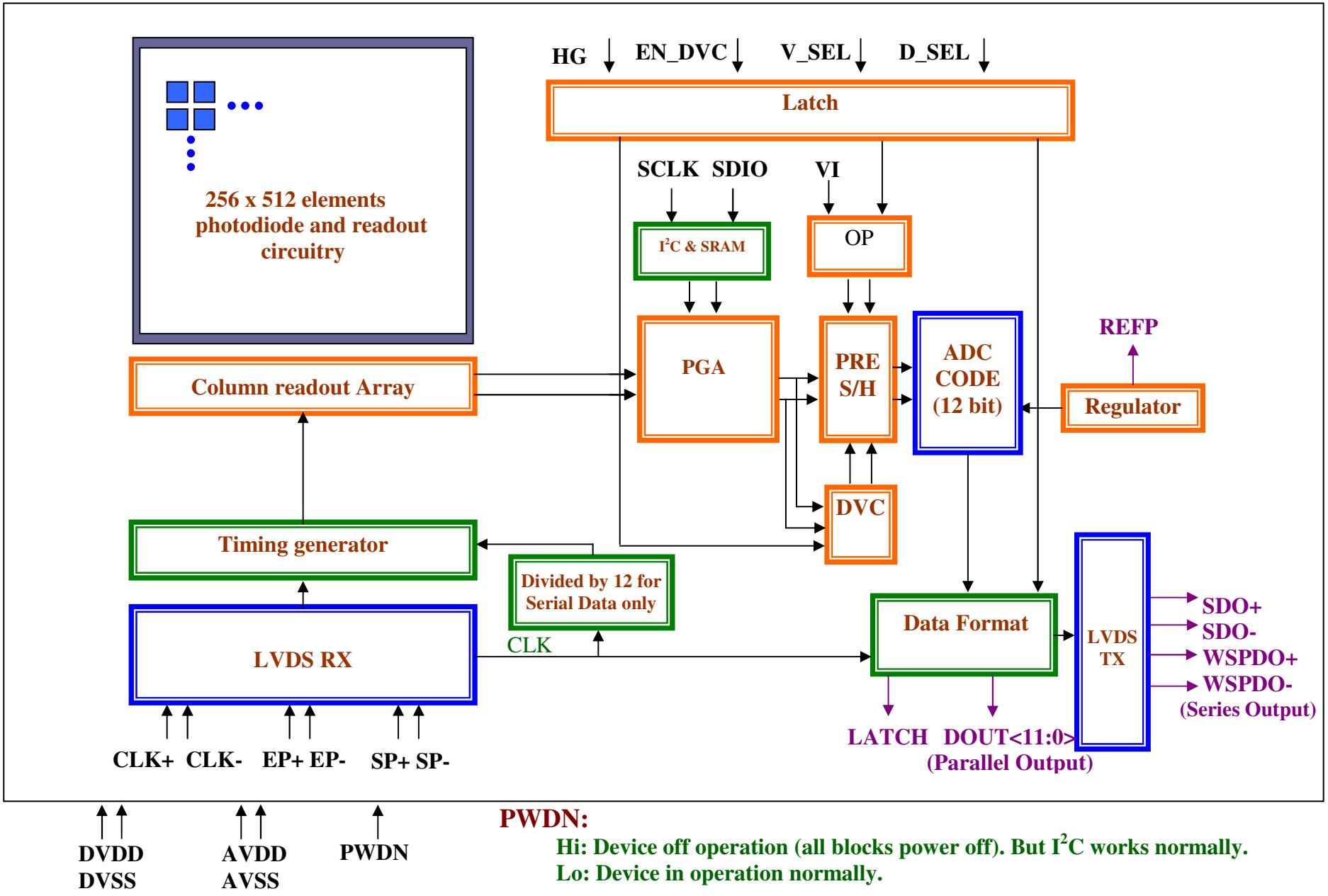


Figure 1. Block diagram of the C650 sensor chip

Based on the device function, the C650 device is separated into (1) sensor stage, (2) gain control and I^2C interface, (3) ADC and reference voltage stage, and (4) input / output control stage. The functionality of each stage is explained as follows.

4.2 Sensor stage

Figure 3 shows the block diagram of the sensor stage. It consists of a 286 x 516 APS array and an in-column buffer driver block that used to isolate parasitic capacitance at APS output line. CMOS Sensor's proprietary advanced active pixel sensor (APS) readout structure is used to converts the charge which accumulated on the photo detector into a voltage signal. This technology provides fixed pattern noise (FPN) suppression and improves the uniformity of the array. CMOS Sensor's proprietary buffer mux technology is also used to readout each pixel signal at each clock rate. The buffer mux circuitry is also performed as a coarse gain control. Since a switch capacitor method is used to build the buffer mux, the linearity is further improved and the fixed pattern noise is further reduced.

4.2.1 Image Sensor Array

The sensor has an active image array size of 256 columns x 512 rows. However, the full array contains 286 columns and 516 rows, with the extra 30 optical block (OB) pixels in each column and the extra 4 OB rows. The optical black pixels are designed to provide a dark reference voltage and eliminate edge effect. For each column, they are arranged for 20 pixels on the beginning of the 1st active pixel and 10 pixels after the 256th pixels. The optical block rows are arranged for 2 rows on the beginning of the 1st active row and 2 rows after the 512th active row.

Figure 5 shows the pixel arrangement of the sensor array and the APS unit. The optical black pixels are same as active image sensor except a light shielding opaque element covers them.

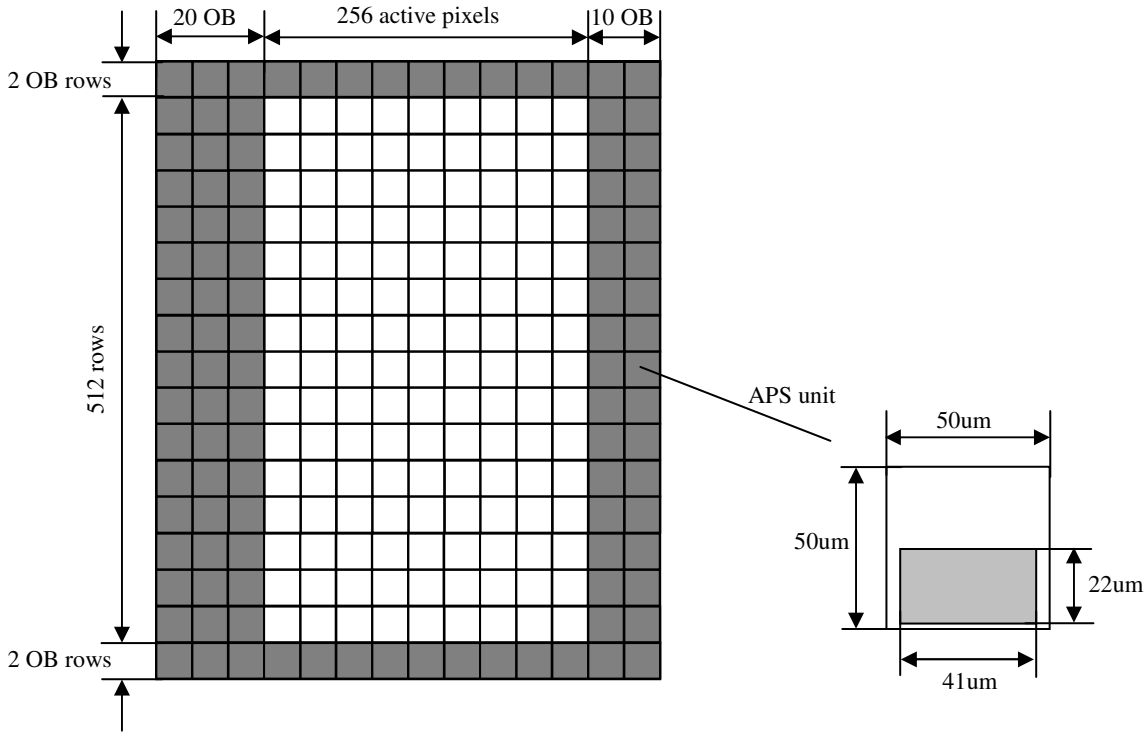


Figure 5. Sensor Array and APS unit geometry

4.2.3. Advanced Charge trans-impedance amplifier (CTIA) readout structure

Figure 8 shows a conventional APS structure. It consists of a photodiode, a reset transistor, a source follower, and a readout switch. When readout switch is turned on, the photodiode voltage will be readout by the source follower. There are, however, several drawbacks on this conventional circuitry approach. The gain of the source follower is always lower than 1 and is non-linear. In addition, the power supply and ground noise are very difficult to prevent on this structure.

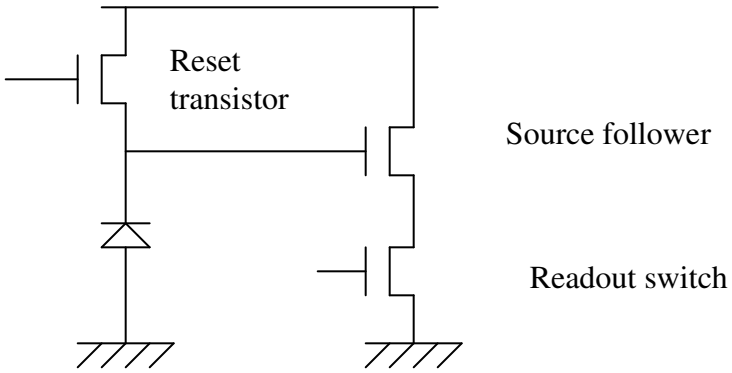


Figure 8. Schematic of conventional APS circuitry

In order to solve this problem, C650 sensor utilizes CMOS Sensor's proprietary advanced Charge trans-impedance amplifier technology. This structure utilizes a charge integrator that provides linearity throughout the full dynamic range. In addition, there is a significant increase in immunity from the power supply and ground noise as compared to the conventional APS circuitry. The gain of the advanced CTIA readout structure is higher and the reset noise is eliminated. The non-linearity is less than 0.08% on the whole video output range.

4.3 Gain control stage

Figure 11 shows the block diagram of the gain control stage. It consists of buffer mux & coarse gain control block, 7-bit programmable gain amplifier (PGA) control block, dark voltage cancellation (DVC) block, and subtract (x2) block. The coarse gain control is used to adjust the global gain of the device while 7-bit PGA is used to compensate the row wise gain. One bit (HG) of the input pin is used to control the coarse gain of x 1 and x 2. The bit word of PGA is controlled through a built-in I^2C interface. This device has an option to select either with dark voltage cancellation or without dark voltage cancellation. The functionality of each block is explained as follows.

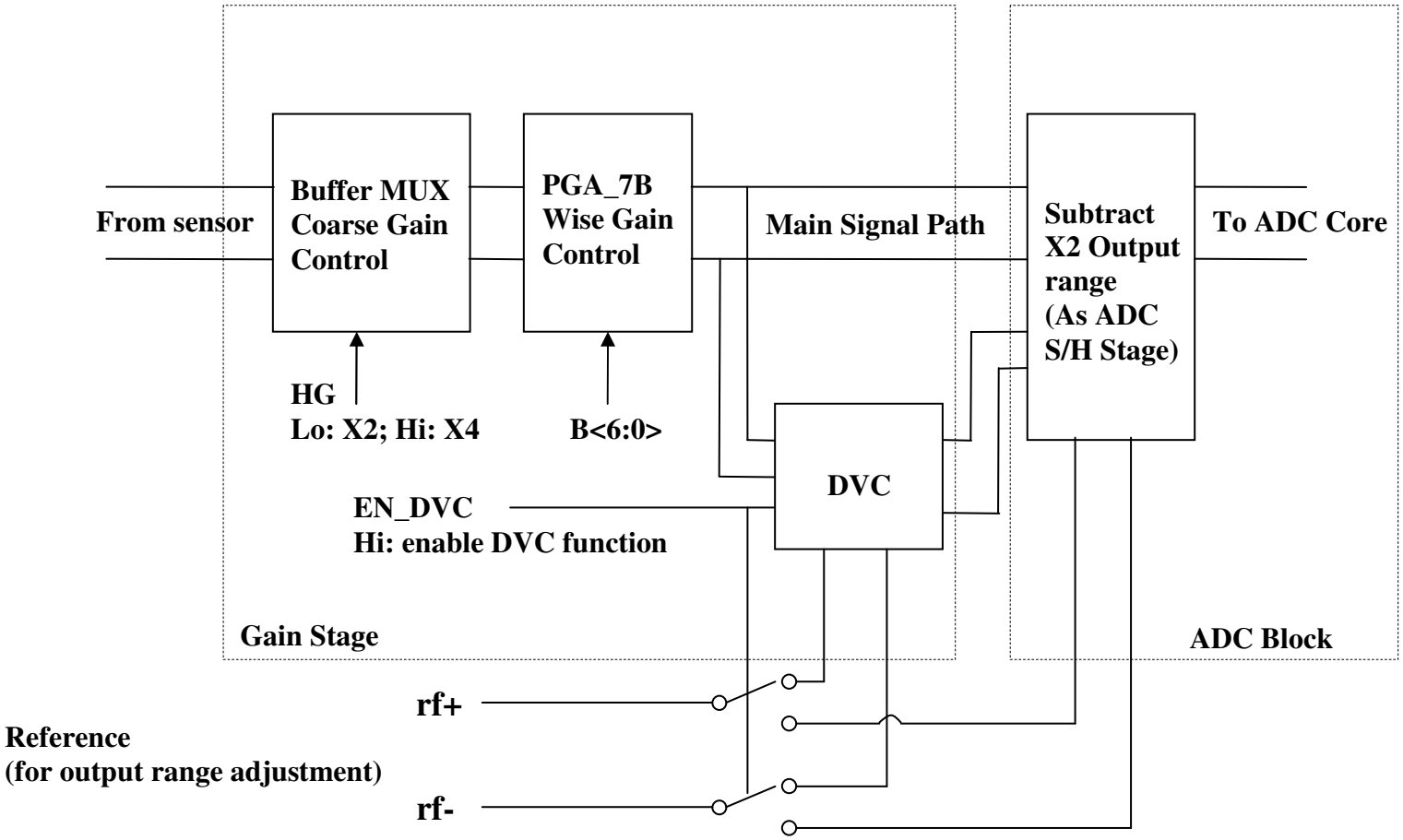


Figure 11. Gain control stage of the C650 device

4.3.1 Buffer MUX and coarse gain control

In the CDS circuitry, each pixel of a conventional readout structure uses two source follower amplifiers. There are several drawbacks to such a source follower approach. Wafer process variation causes a variation in the gain and offset for each source follower resulting in a significant fixed pattern noise problem. In addition, the gain of the source follower is less than one.

For this design, we will use a charge integrator to convert the pixel signal. Since all of the signals go through this single charge integrator, the fixed pattern noise is eliminated. In addition, the amplifier on the charge integrator utilizes a dual differential amplifier to eliminate both power supply noise and ground noise.

The coarse gain applying to Buffer Mux is controlled by an external pin (HG). The gain control table is shown in table 2. The non-linearity is less than 0.02% for the whole voltage range.

4.3.2 Row wise PGA gain control

PGA set the row wise gain of each row for spectral response compensation through I^2C interface. A switch capacitance technique is used on the PGA block. Figure 14 shows the schematic of PGA. The transfer function at output mode is shown as follow.

$$V(out) = -\frac{C(2^0 b_0 + 2^1 b_1 + ... + 2^{n-1} b_{n-1}) + C_0}{Cf} * V(in)$$

The row wise gain range of PGA is settable from x1 (for all bit words are low) up to x5 (for all bit words are high), based on the typical row wise response curve. The linearity characteristics for all operation conditions are show in figure 15. The non-linearity is less than 0.1%.

4.3.3 Dark voltage cancellation circuitry

The charge (Q_d) generated from dark current on the opaque pixel is shown as follows:

$Q_d = I_d * T_{int}$

Where I_d is the dark leakage current on the opaque pixel, T_{int} is the integration time.

The charge (Q) generated from active pixel is shown as:

$Q = (I_L + I_d) * T_{int}$

Where I_L is a light current generated from incident light. I_d is the dark leakage current on the active pixel.

The dark voltage on the opaque pixel is the same as active pixel. By clamping the DC voltage on the opaque pixel, the dark leakage current is subtracted. The video signal on the output of the dark voltage cancellation circuitry is the real video signal that is generated from incident light. A simplified block diagram of the dark voltage cancellation circuit is shown in figure 16.

GAIN	HG
X 2	0
X 4	1

Table 2 The coarse gain control table

- Spectral response compensation is performed through a 7bit PGA device
- PGA gain for each row is settable in a memory using I^2C interface

Row Wise Gain Control (Gain Range: x1~x5)

Transfer function:

$$V(out) = -\frac{C(2^0 b_0 + 2^1 b_1 + ... + 2^{n-1} b_{n-1}) + C_0}{Cf} * V(in)$$

Gain Setting:

<b:0> all low: gain=1

<b:6> all high: gain=5

Linearity properties:

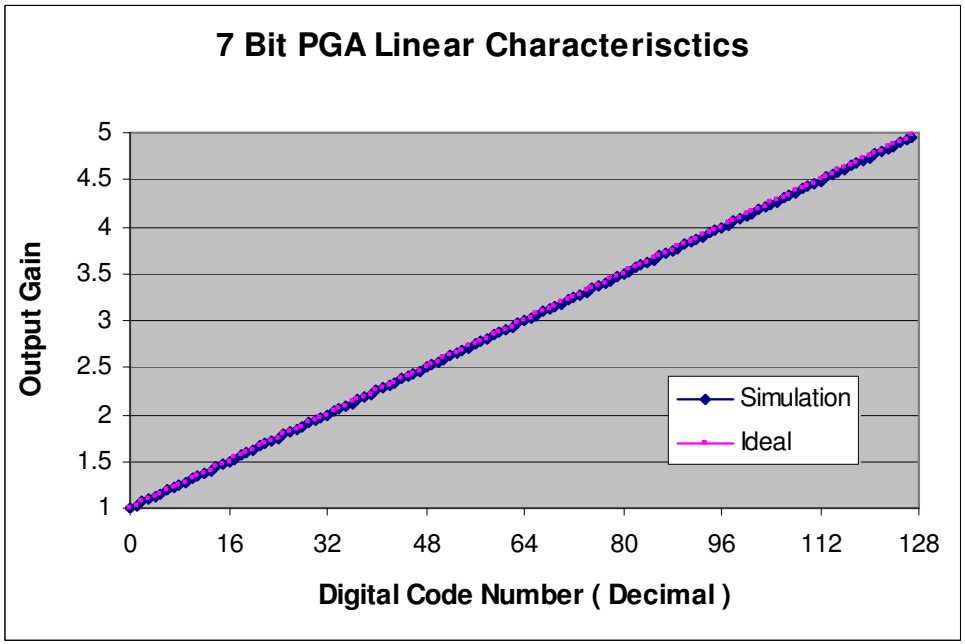


Figure 15 PGA transfer function, gain setting range and linear properties

4.3.4 I²C Interface

This block is used to set the row wise PGA gain for each row to a memory. There are preset power-on default gains in the memory. I²C is designed to be able to read out these preset values and device setting values, such as coarse gain, ADC input selection, data output type selection and operation status (power on/off) etc. It always is active whatever in imaging and power down mode.

Figure 17 shows top level I²C block diagram. It contains two portions: one is standard I²C interface and the other one is a SRAM memory block. I²C block performs three operation modes:

Write mode: set row wise gain value for each row to memory and load to PGA gain control block;

Read mode: register read out for current device setting values, such as HG, V_SEL, etc.

Power ON mode: load the default row wise gain value of memory to PGA gain control block.

I²C bus protocol and AC waveforms is shown Figure 18 and Figure 19 respectively. Figure 20 and 21 describes the register address. The operation sequences for write/read mode are shown in Figure 22 and Figure 23 respectively.

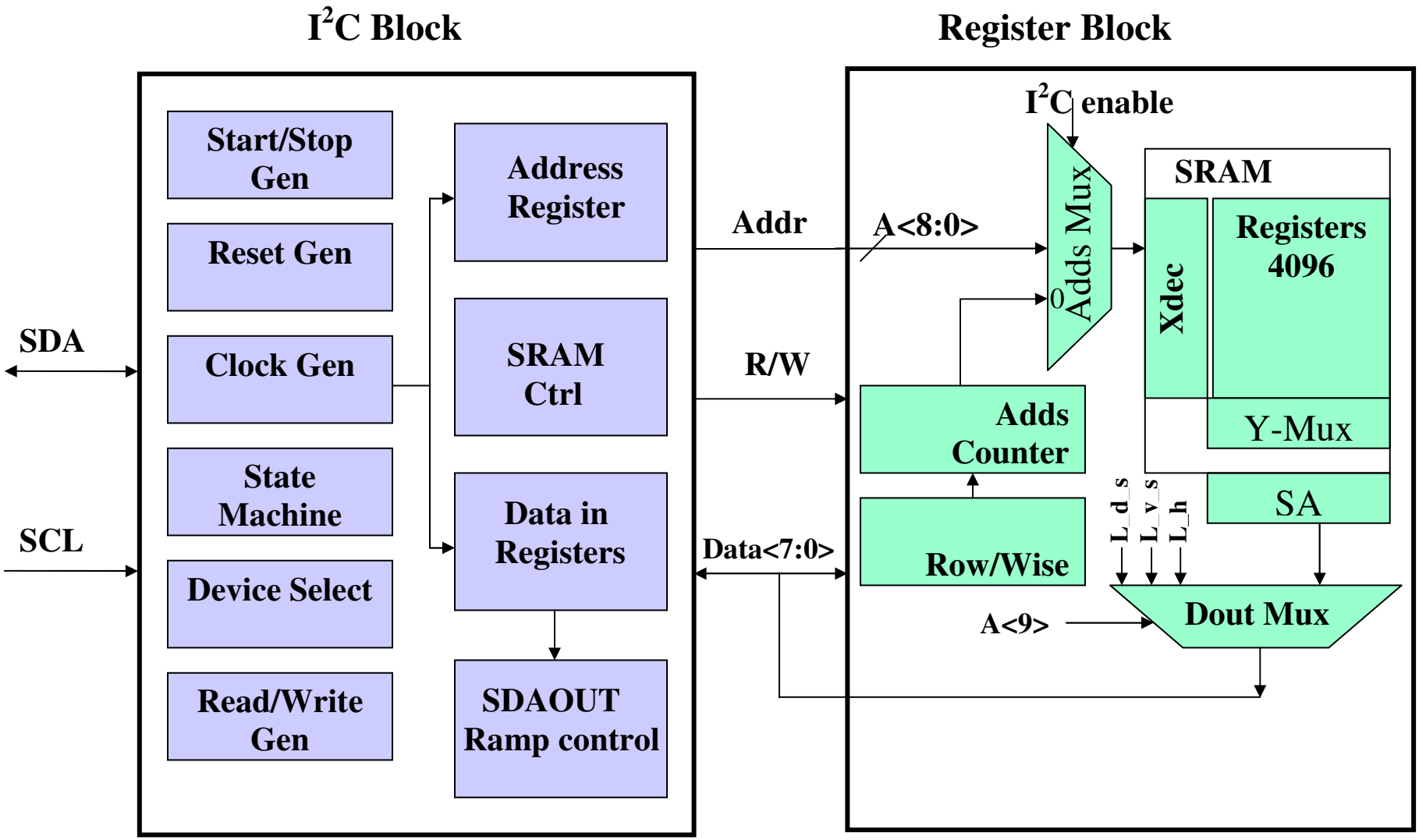


Figure 17. The top level I²C block diagram

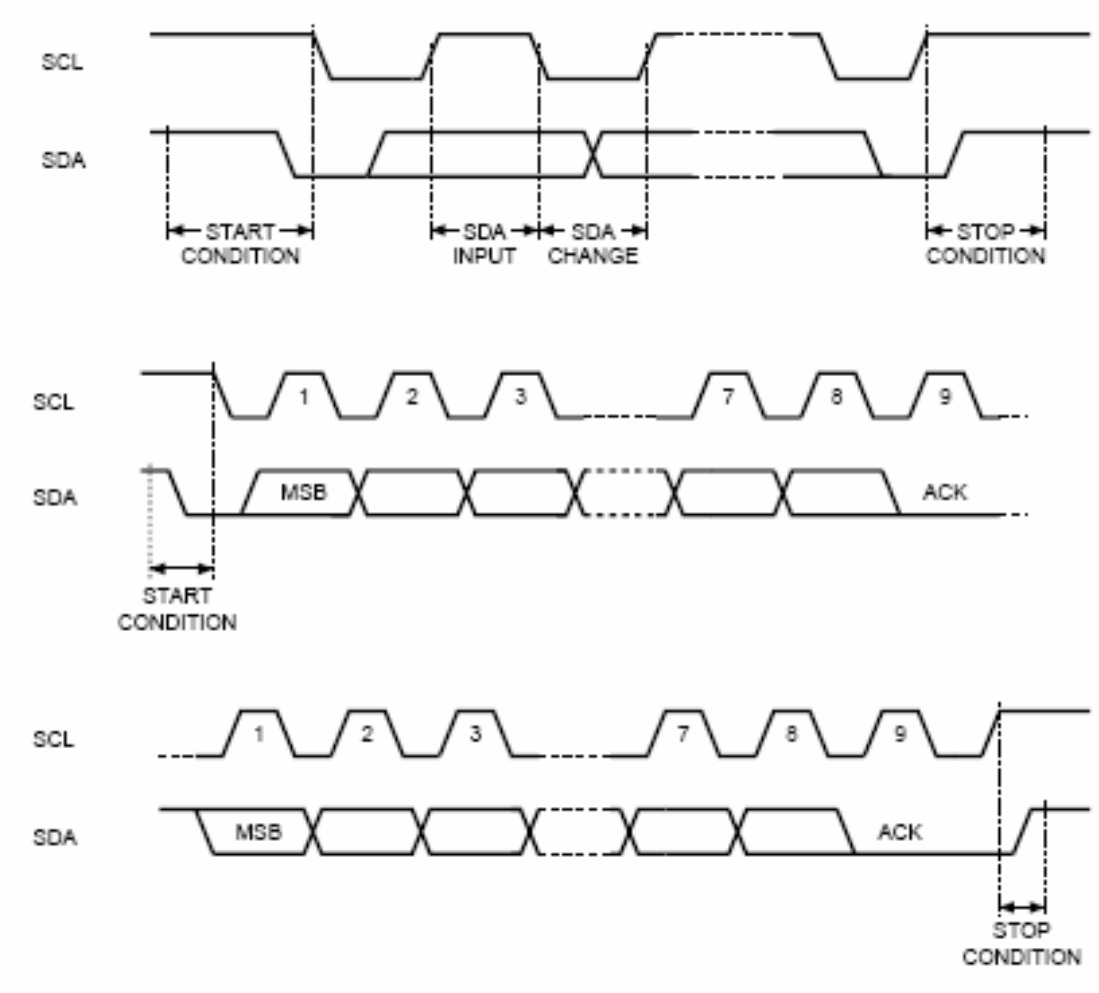


Figure 18. I^2C bus protocol

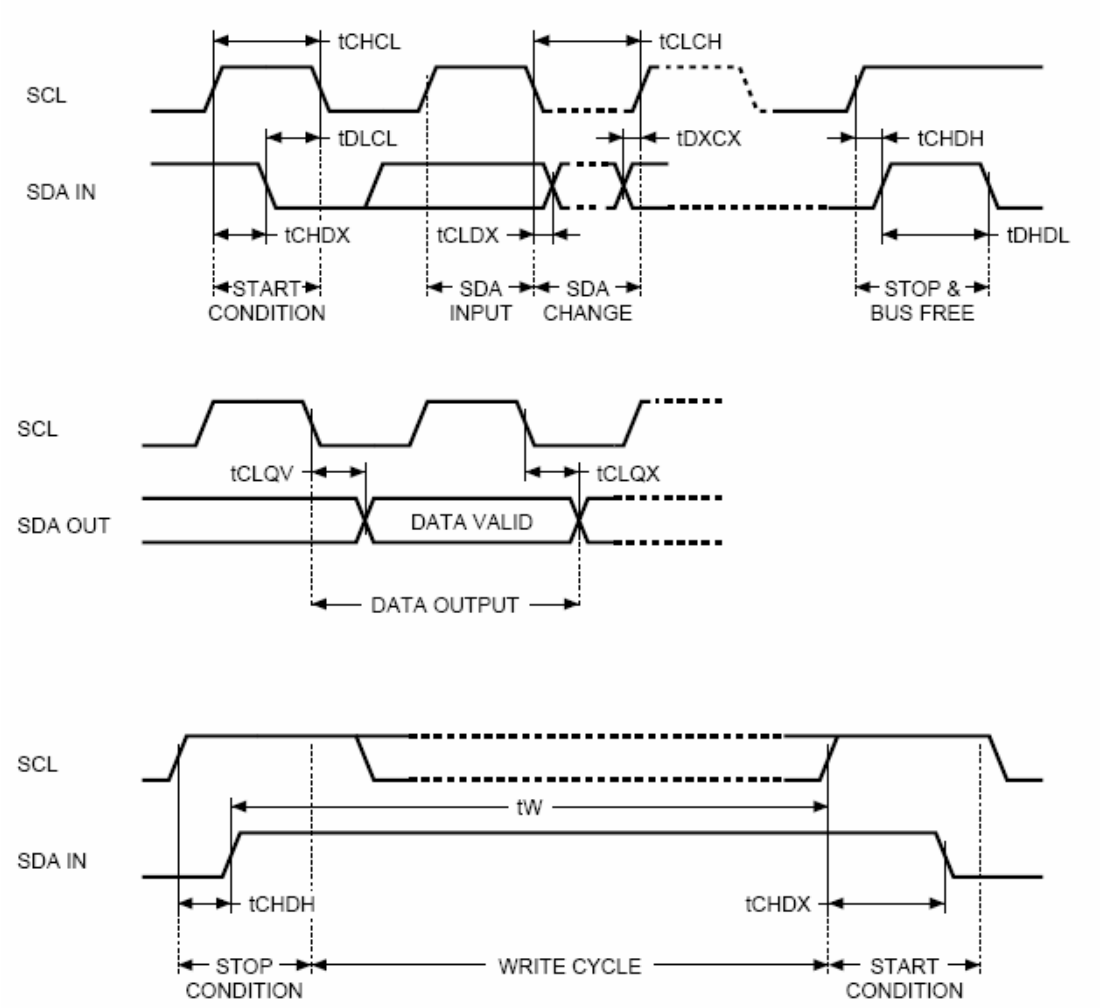


Figure 19. AC waveforms

Device Select Code

	Device Code				Chip Enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	0	0	0	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 2.2.1

Operating Modes

Mode	$R\overline{W}$ bit	$\overline{WC}$	Data Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X	1	START, Device Select, $R\overline{W}$ = '0', Address,
	'1'	X		reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	≥ 1	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IL}	1	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	≤ 64	START, Device Select, $R\overline{W}$ = '0'

Note: 1. X = V_{IH} or V_{IL}.

Table 2.2.2

Figure 20. Register address: first byte ---- device select

Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

b15 is don't care on M24256 series.
b15 and b14 are don't care on M24128 series.

Least Significant Byte

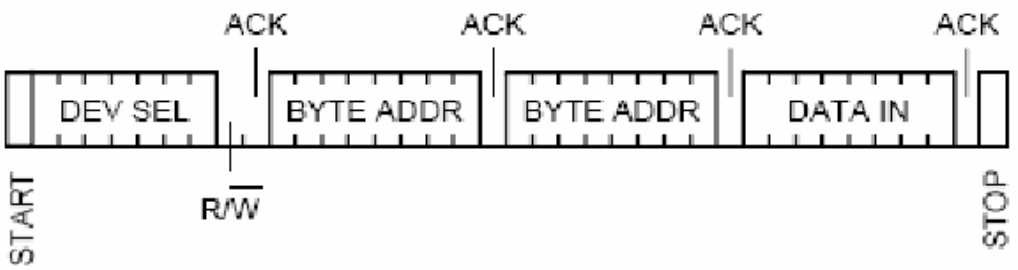
b7	b6	b5	b4	b3	b2	b1	b0

Note: A<15:10> don't care for Register Address
A<9> = 0 for SRAM address
A<9> = 1 for 5 bits read (HG, V_SEL, D_SEL, EN_DVC and PWDN)

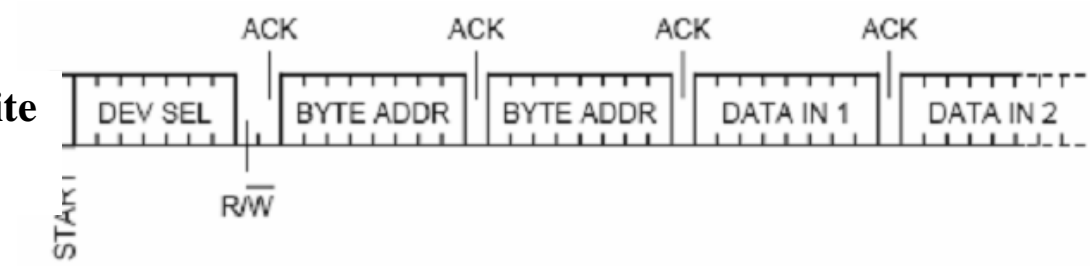
Figure 21. Register addressing: ---- Upper Address first, then Lower Address

- Write Modes Sequences

Byte write



Sequential Write



Sequential Write (cont)

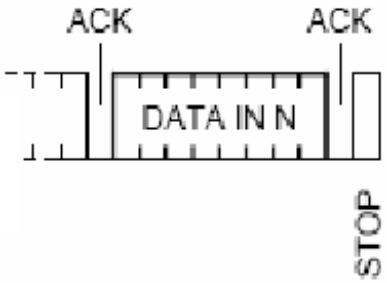


Figure 22. Operation sequences for write mode

- Read Modes Sequences

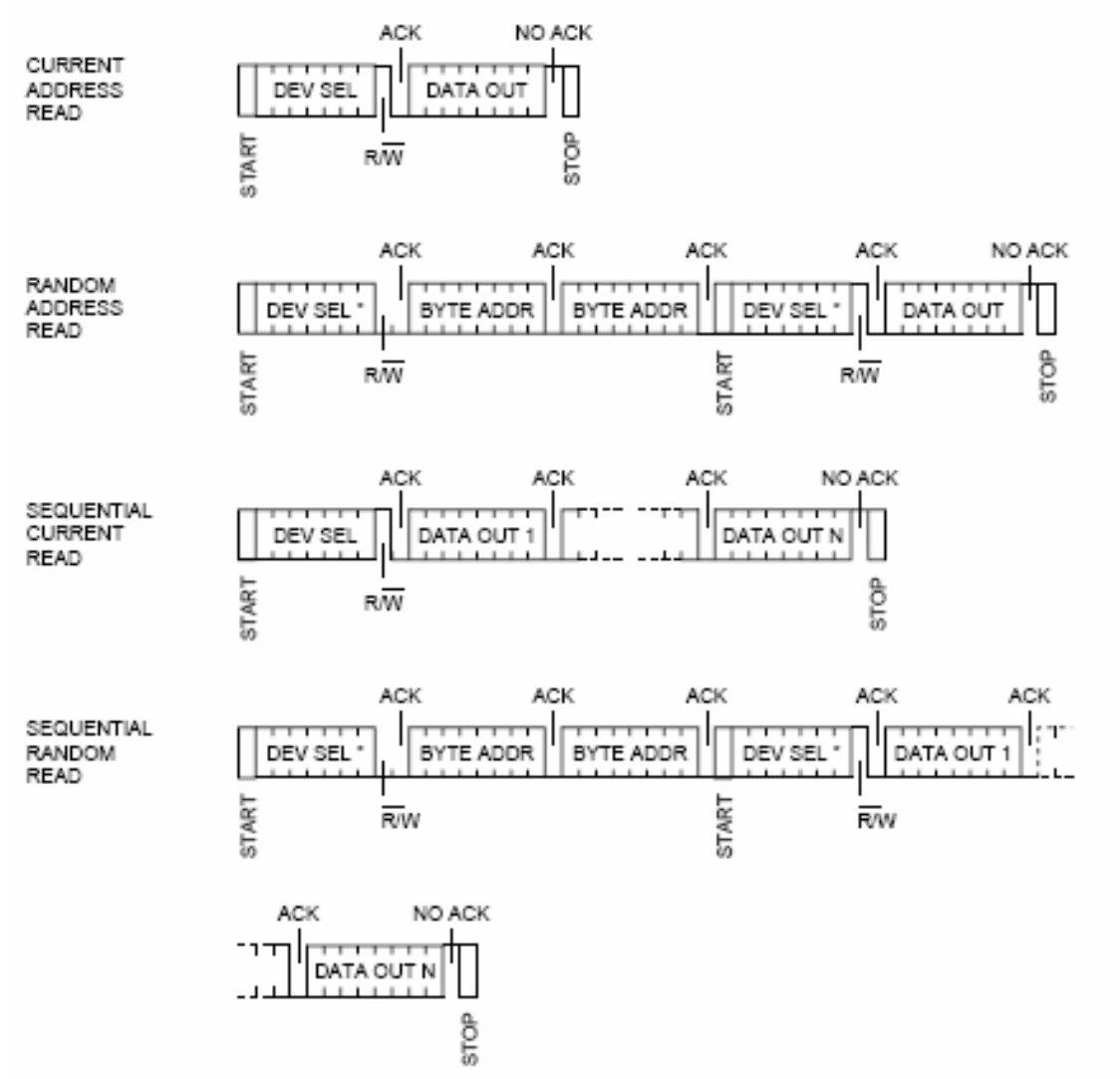


Figure 23. Operation sequences for read mode

4.4 Analog to Digital Converter (ADC) and reference voltage generator

A 12 bit of the pipeline Analog to Digital Converter (ADC) is used to convert from analog signal to digital data output. Figure 24 shows the block diagram of the 12-bit ADC and reference voltage. A pipeline ADC structure is used to design 12 bit ADC since its high speed and high performance characteristics.

The band gap and reference voltage block support the reference voltage of the ADC block. This reference voltage will provide a very stable voltage to the ADC. When either temperature is changed or the power supply voltage is changed, the reference voltage is still keep constant. It is very important for the ADC. The reference voltage of the ADC is normally adjusted to maximum 2.048 V. This value represents the full scale of the ADC input range.

In order to test the performance of the ADC, an external V_{in} bonding pad and a multiplexing switch is used. An input saw-tooth waveform is then applied to the ADC. By comparing the waveform of the analog input and digital output data, any missing code after the ADC can be detected. In the normal operation mode, the output from PGA is connected to the input of the ADC.

4.4.1 12-bit ADC

Figure 25 shows a system block diagram of the 12-bit ADC converter. It consists of (1) a pre sample / hold, (2) a 12-bit pipeline ADC core and (3) a digital correction output buffer. The 12-bit pipeline conversion core consists of 11 conversion 1.5-bit stages and 1 conversion 1-bit stage, as shown in figure 26. There is a total of 23 bit of the digital output from 12bit conversion core. The detailed function block diagram of the 1.5 bit stage is shown in figure 27. The conversion algorithm is shown in figure 28. The spice simulation of MDAC transfer function for the input differential voltage from – 2.048 V to 2.048 V is described in figure 29. Figure 30 presents the transfer error for the whole voltage range. As shown in the figure, the error is less than 0.5 LSB. The setting time for three different simulation conditions (typical, best and worst case) for low voltage, middle voltage, and high voltage is displayed in figure 31. The performance of the ADC is presented in table 3. This circuitry is used on our standard product. The pipeline ADC can achieve high speed, high performance and low noise for this application.

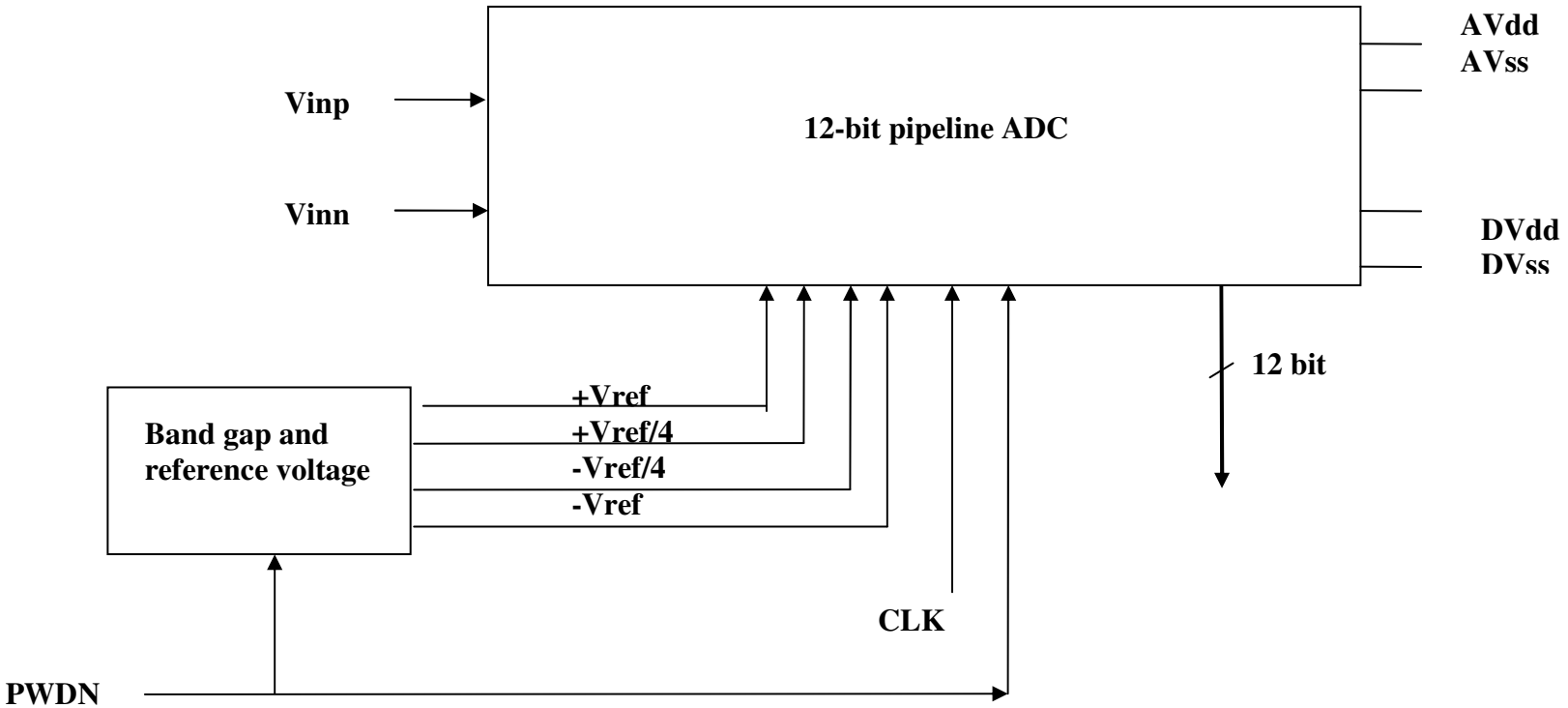


Figure 24. Block diagram of the 12-bit ADC and reference voltage

• Block Diagram

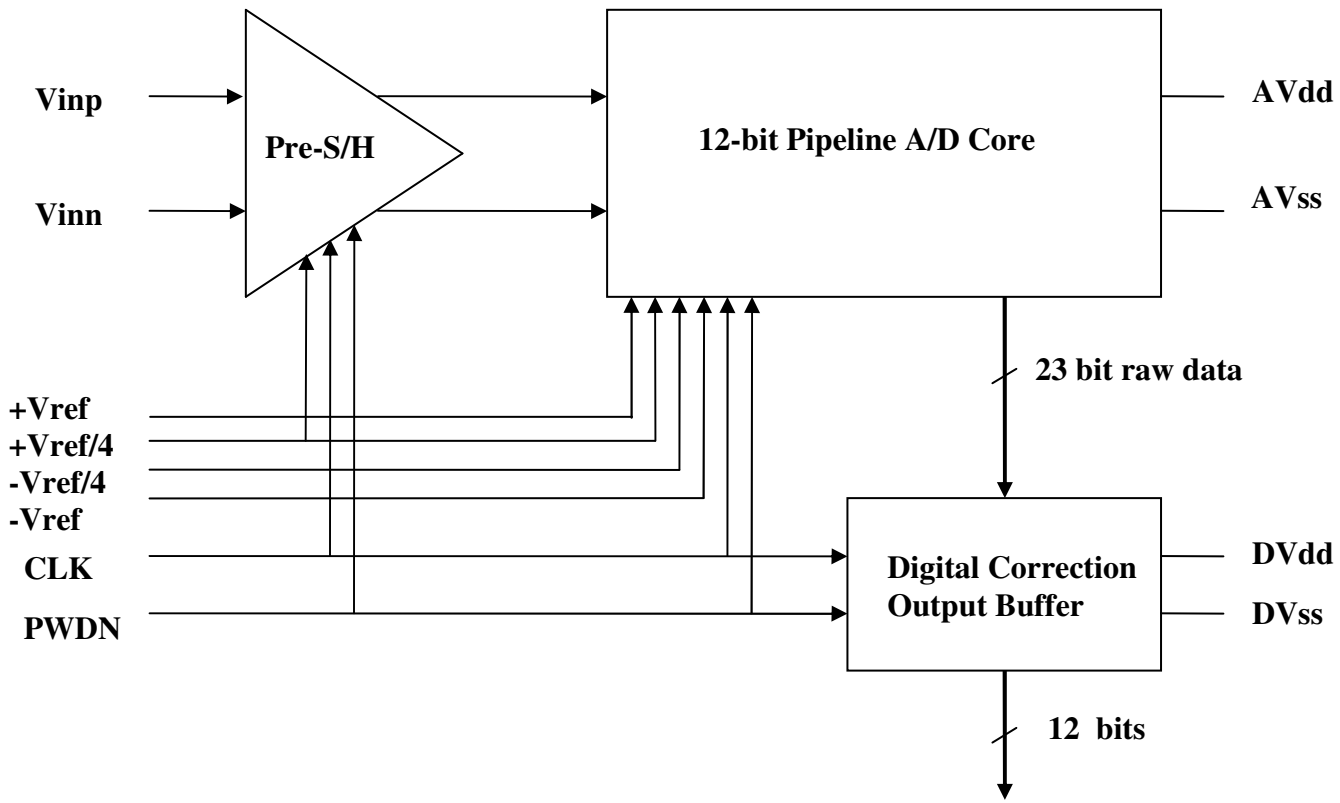


Figure 25. Block diagram of the 12-bit ADC

Block Diagram

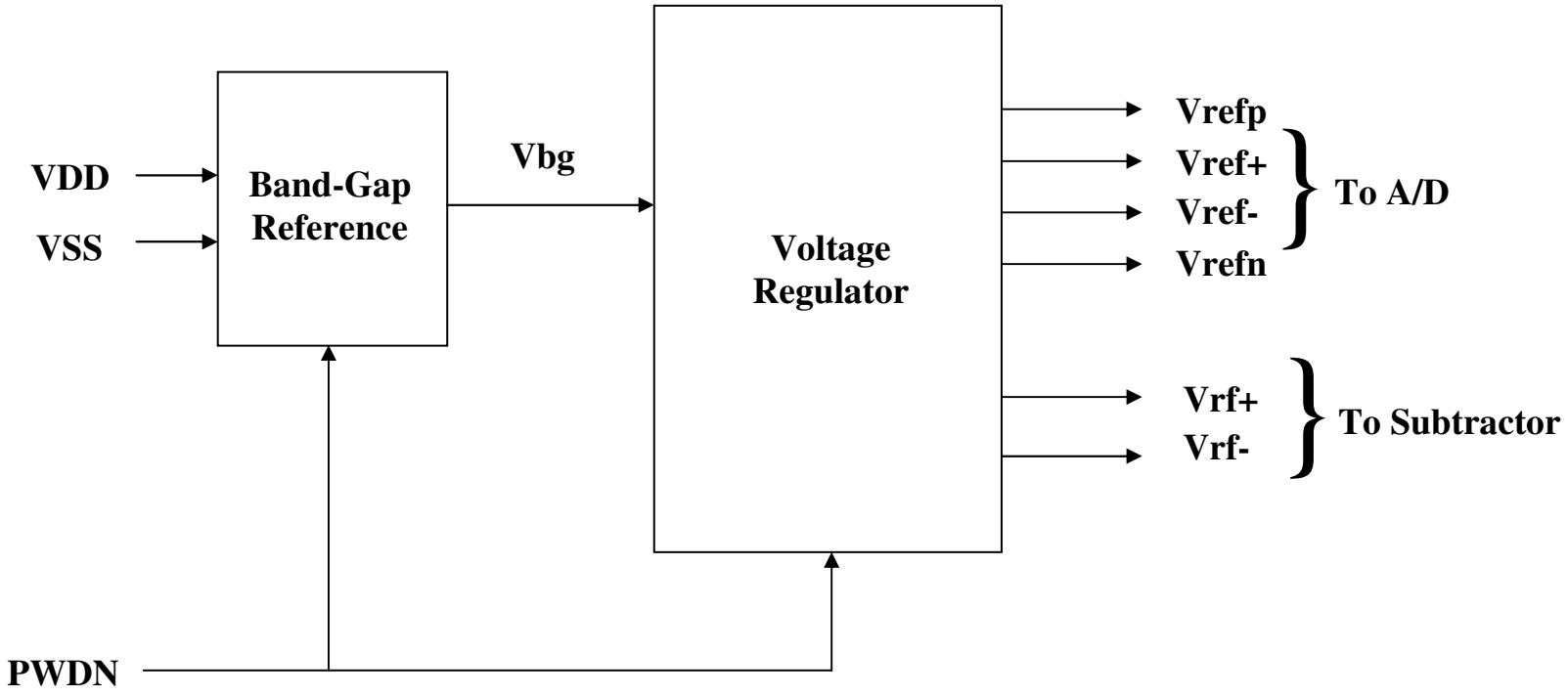


Figure 32. Block diagram of the reference voltage

4.5 Input and output stage

This stage consists of (1) data input control, (2) data output control, and (3) external analog input voltage control. The functionality of each control will be explained in the following.

4.5.1 Data input control

Figure 34 shows the block diagram of the data input control. It consists of (1) LVDS receiver block, (2) latch block, (3) I2C interface, (4) Timing generator. All of the timing to operate the device is generated from divided by 12 and timing generator block.

4.5.1.1 Timing Generator

Only three input clock pins are required for this device. One is master clock (CP, 36 MHz for serial data output and 6 MHz for parallel output); second is a synchronized clock start pulse (SP) and third is exposure control pulse (EP). The master clock and start pulse generate pixel clock pulse (PCK) and initiated start pulse (SP0). The timing generator block provides the logic circuitry to operate this device. It controls the following functions.

- Image sensor array control and two operation modes (imaging and power down mode).
- Provide the timing for the readout circuitry
- Provide the timing for Auto exposure control, dark voltage cancellation, and gain control
- Provide the timing for ADC and data format
- Provide the timing for row wise gain loading via I^2C
- External output timing (SDO and WSPDO)

4.5.1.2 LVDS Receiver block

Figure 35 shows the block diagram of the LVDS receiver block. The differential LVDS input clock pulse converts from differential input pulse to the CMOS clock pulse. Three input clock pulse (CP, SP, and EP) is applied to the device. Those three input clock pulse connected to timing generator block to generate all necessary clock pulse to operate sensor, gain stage and ADC etc.

4.5.1.3 Power ON default setting

All default digital settings except PWDN is loaded by the power ON reset circuitry (POR) as shown in Table 4. The PWDN is independently controlled by the digital settings at the PWDN pin (imaging mode PWDN=0 (default) and power down mode PWDN=1).

Coarse gain HG is loaded by the LSP (width > 5ck). EN_DVC, D_SEL and V_SEL is loaded at the start of every frame with SP0. Row wise gain values is loaded though I^2C

Input pin name	Value	Description
HG	0	Coarse gain = 2
V_SEL	0	External input disable
D_SEL	0	Parallel data output mode
EN_DVC	0	Dark voltage cancellation disable

Table 4. Power ON default setting value of the C650 device

4.5.2 Data output control

C650 provides two types of data format: serial data output and parallel data output. D_SEL is the data format selector. Figure 36 shows the block diagram of the data output control. It consists of (1) data format block, and (2) LVDS transmitter block. The data format block either output the 12-bit parallel data from ADC block if D_SEL is at low or converts this parallel data to serial format if D_SEL is at high. The data is then go thru LVDS transmitter to convert to the LVDS differential clock pulse.

4.5.2.1 LVDS Transmitter (TX) block

Figure 37 shows the block diagram of the LVDS TX block. The single end CMOS input clock pulse converts from CMOS clock pulse to the differential clock pulse. There are two clocks pulse data output (SDO and WSPDO). The SDO is a serial data output; and the WSPDO is a word start pulse for each data output.

4.5.3 External input voltage control

In order to test the ADC performance, an external input voltage control is applied to the ADC. Figure 38 shows the block diagram of the external input voltage control. It consists of one single end to

differential converter. When V_SEL is low, the ADC input is come from gain control stage. When V_SEL is at high, the ADC input is connected to the external input voltage.

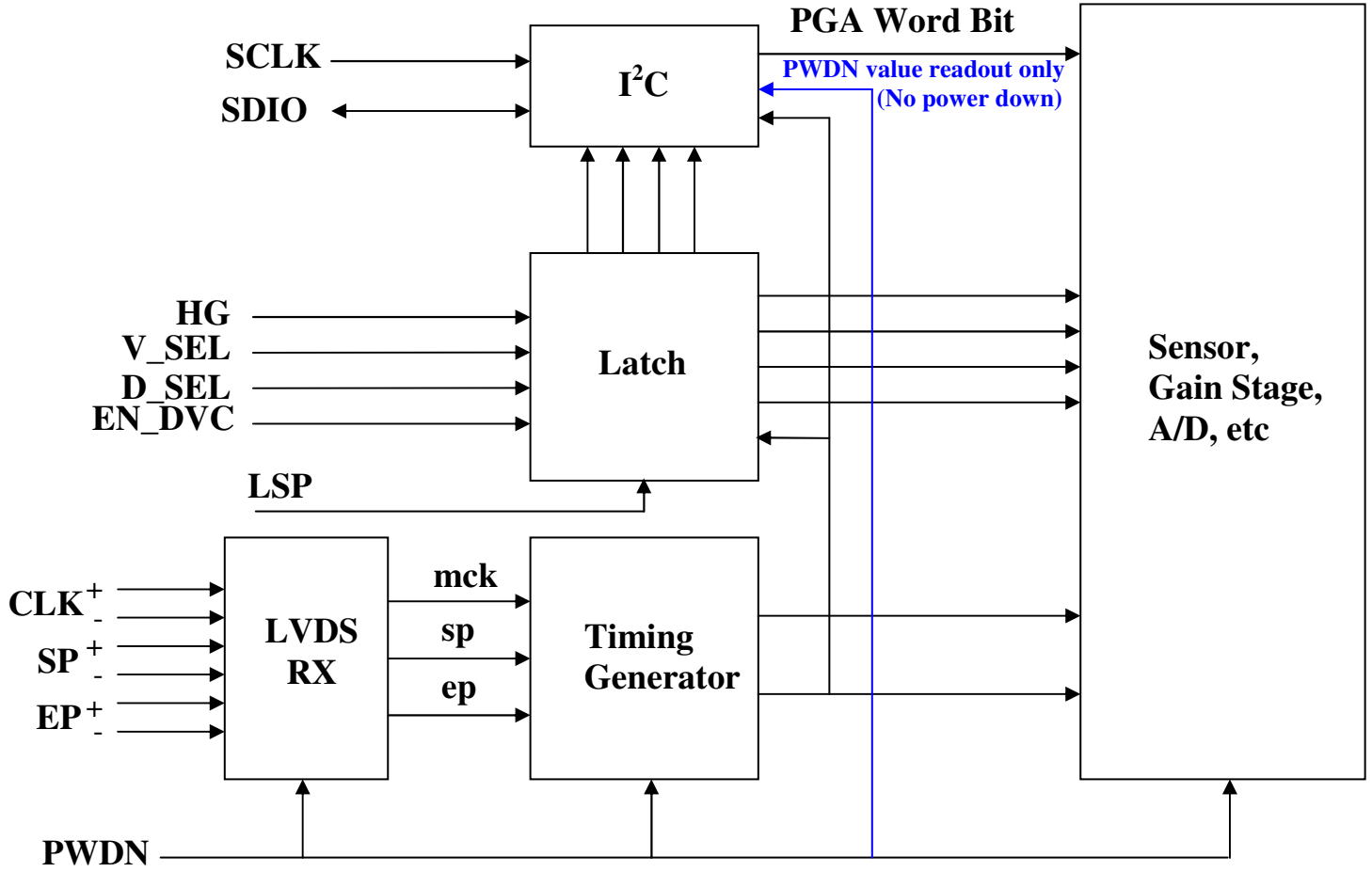


Figure 34. Data input block diagram

LVDS_RX

- Receive master clock, start pulse, exposure control signal and output to system

- Block Diagram

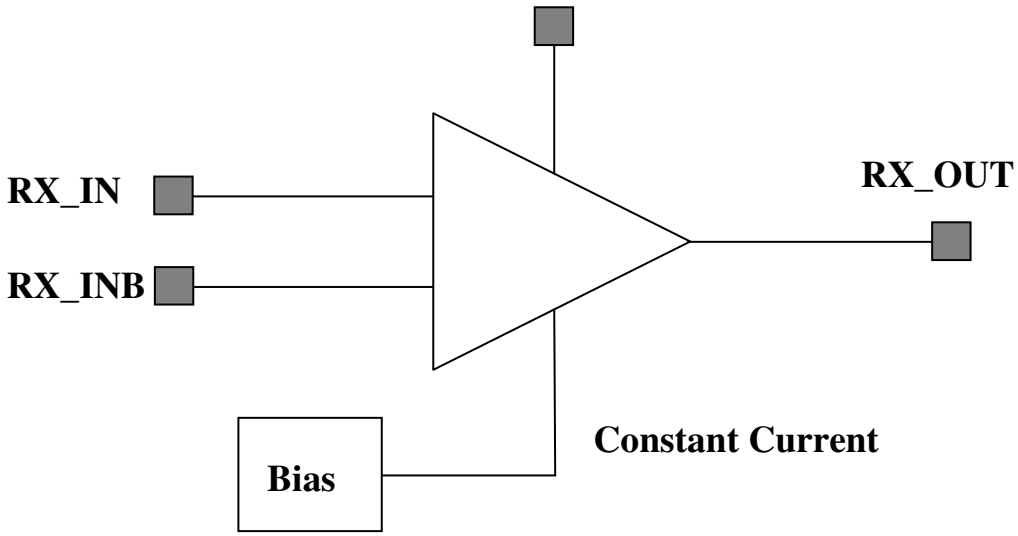
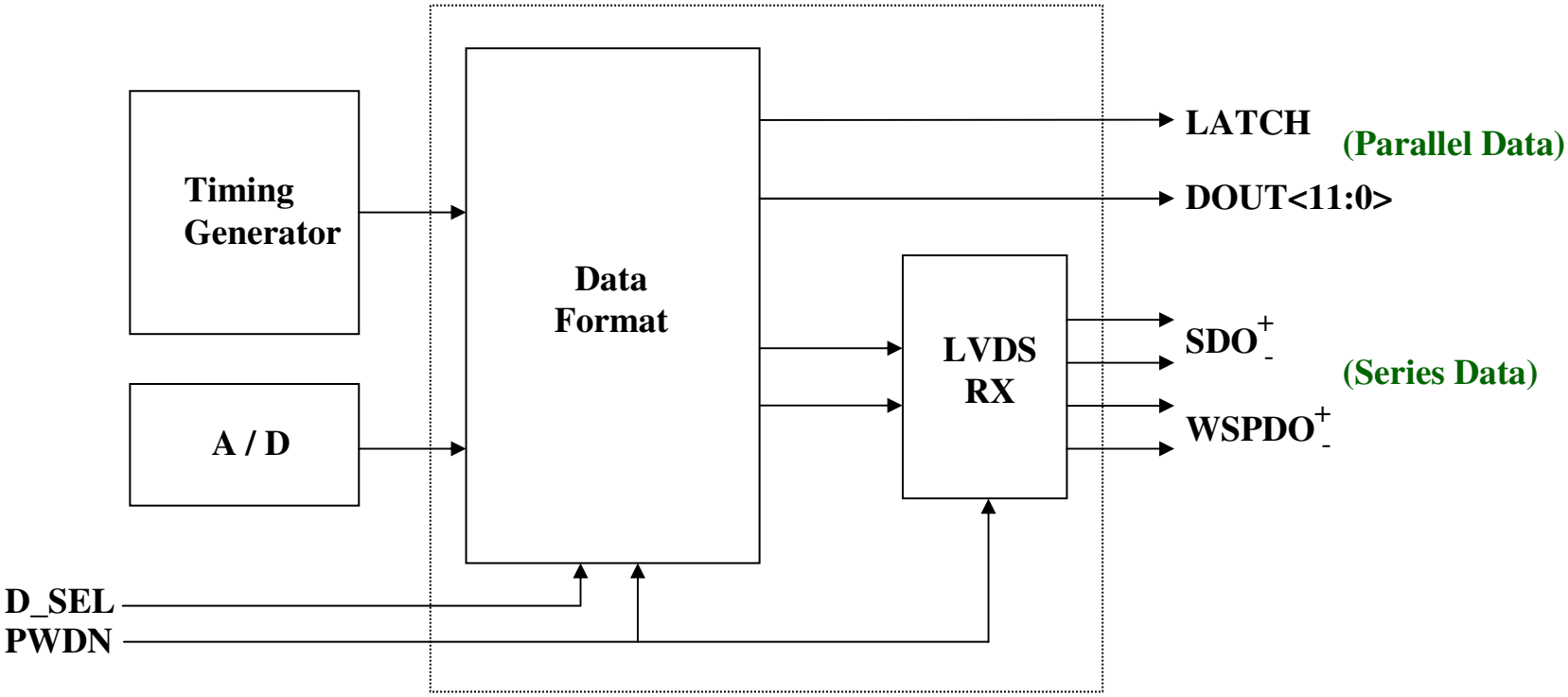


Figure 35. Block diagram of the LVDS_RX



D_SEL Lo: LATCH and DOUT<11:0> active; SDO±, WSPDO± disable
Hi: LATCH and DOUT<11:0> disable; SDO±, WSPDO± active

Figure 36. Block diagram of the Data output control

LVDS_TX

- Series Data Output through LVDS Transmitter
- Block Diagram

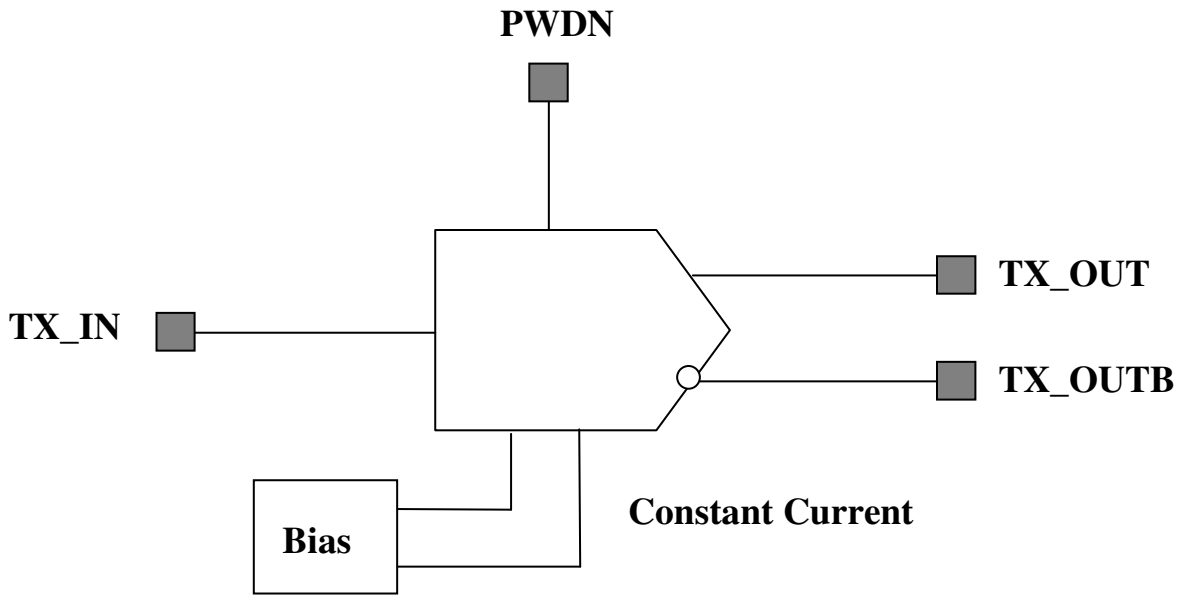


Figure 37. Block diagram of the LVDS_TX

External input voltage control

- For A/D Testing

  Testing voltage sampled in through a single-end to differential voltage converter

Control Pin

- V_SEL Hi: for Testing
  Lo: for Function Disable

Block Diagram

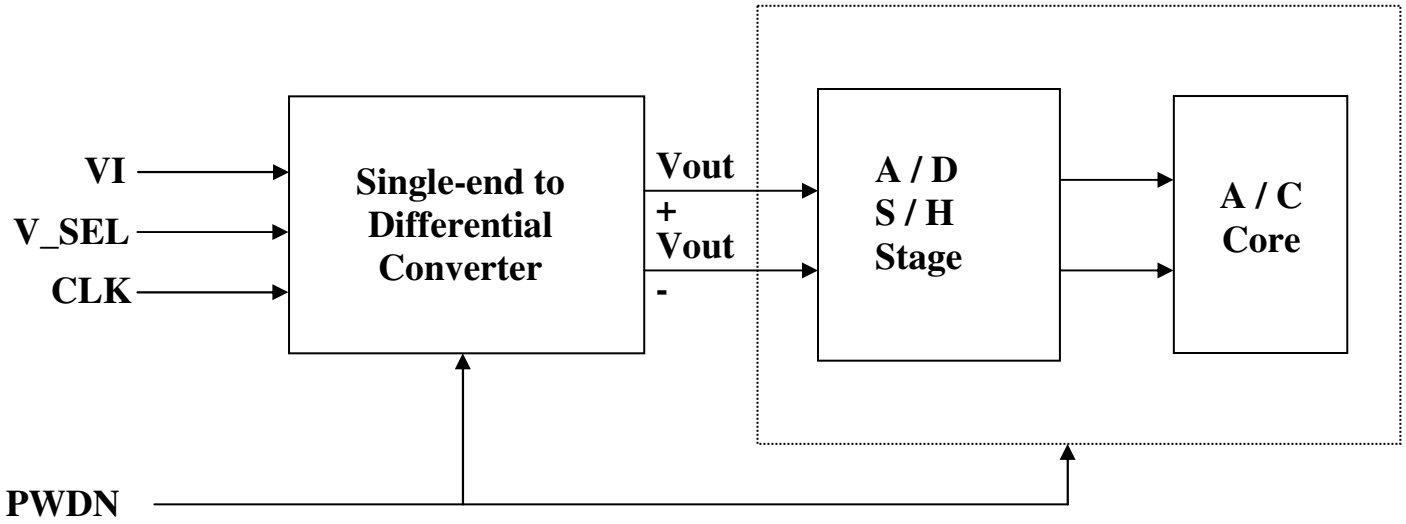


Figure 38. Block diagram of the external input voltage control

5. ELECTRIC CONFIGURATION AND EXTERNAL INTERFACE

5.1 Timing diagram

5.2 CMOS input / output electrical characteristics

5.3 LVDS TX and RX electrical characteristics

5.4 Duty Cycle, gate capacitance, gate structure and V-I characteristics for all clocks and data input lines

External Interface

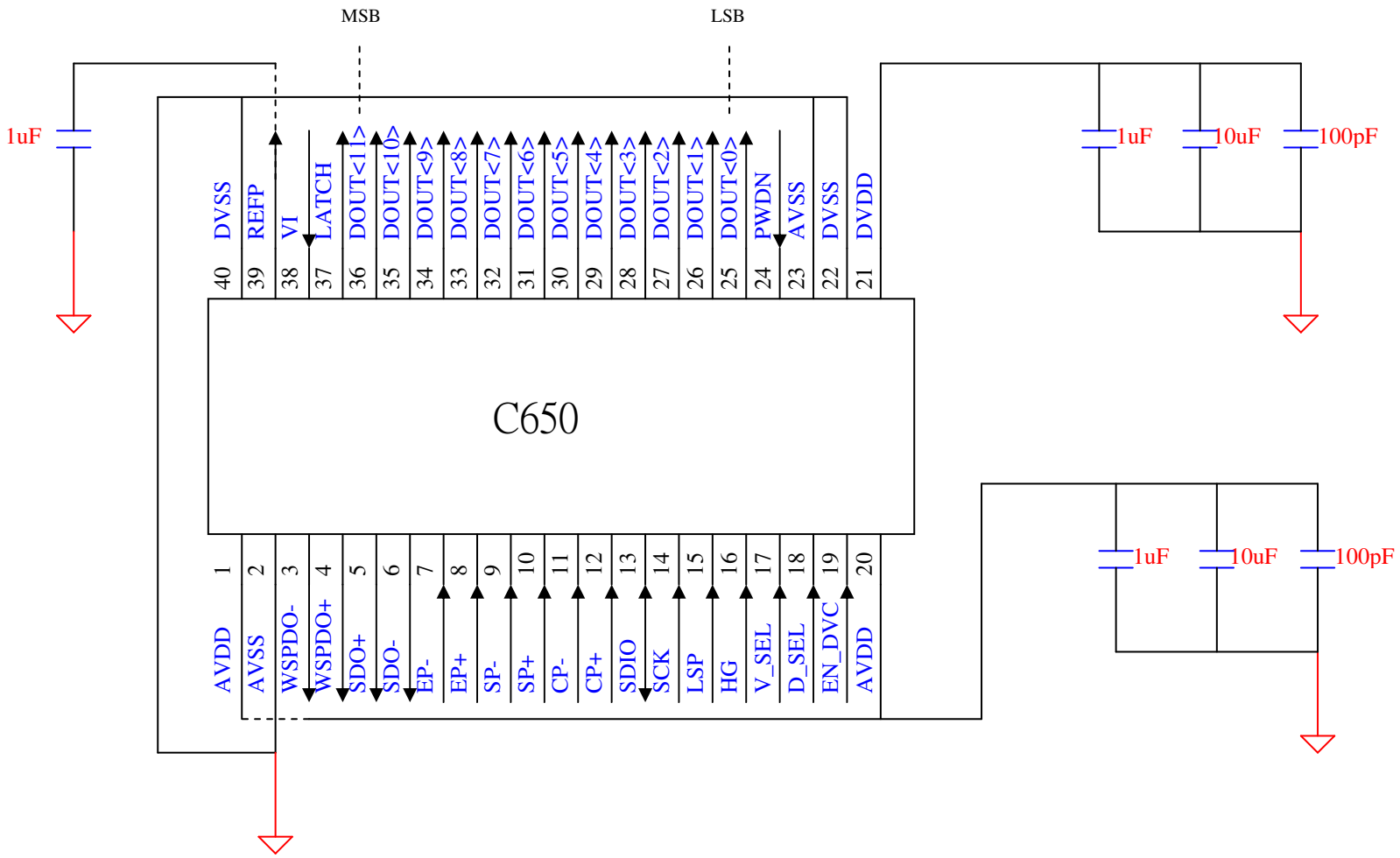


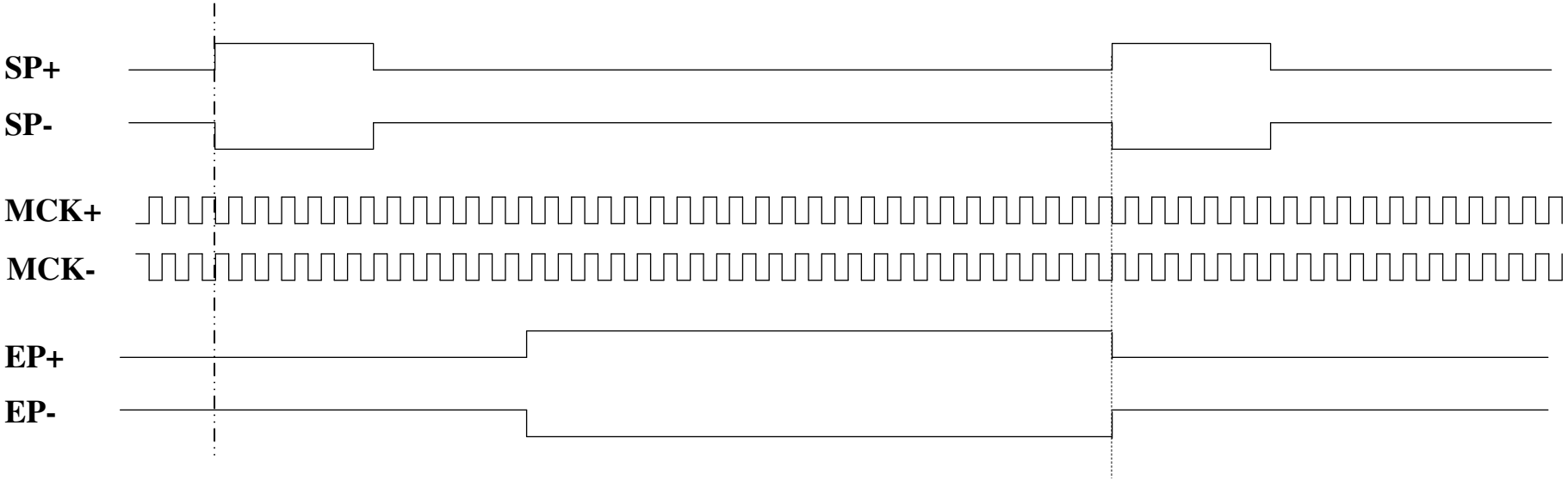
Figure 39. External interface of the C650 device

■ Timing Diagram

(External Signals for Parallel Output and Serial Output Mode)

- **Differential Input Clocks (to LVDS_RX)**

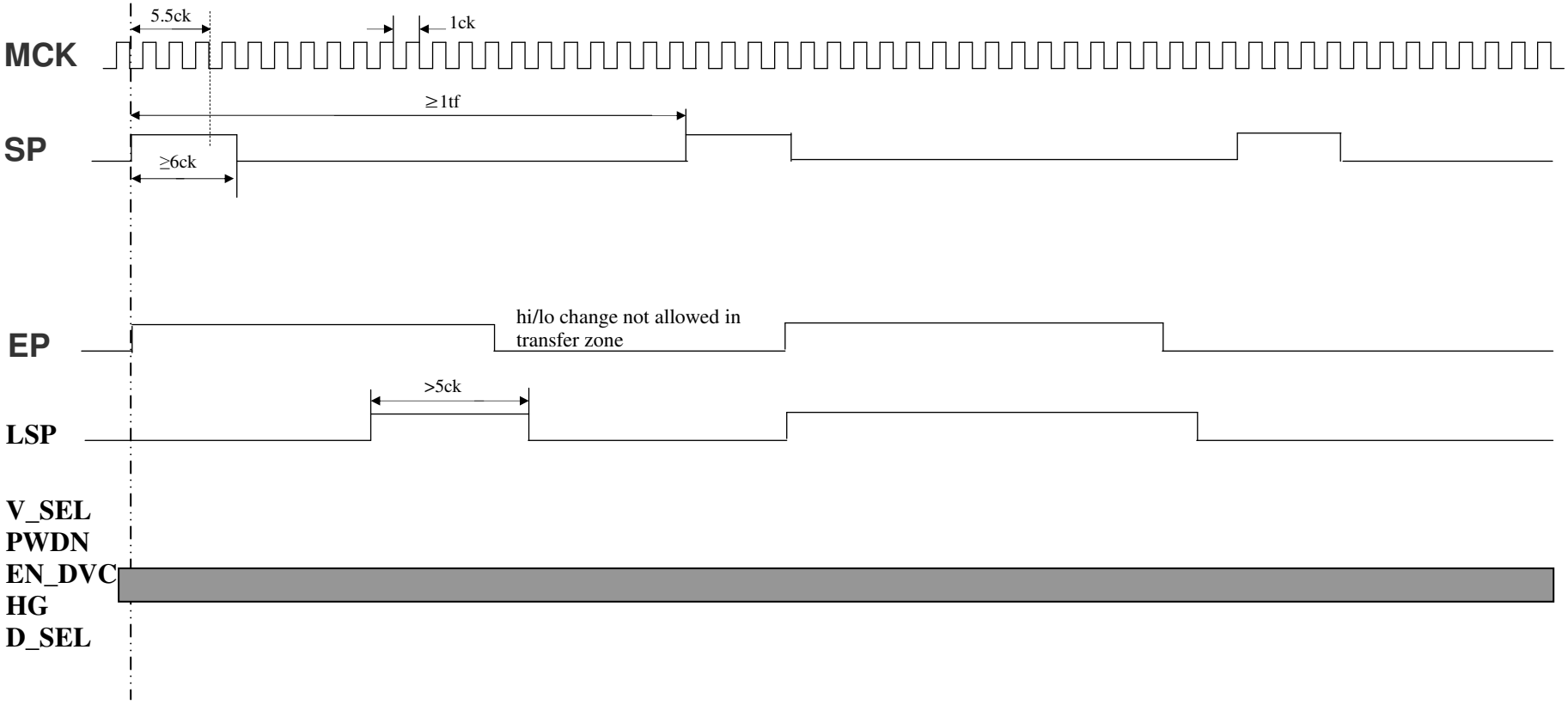
For Fr=20frames/s, for parallel output, input frequency = 2x3.061MHz, 1ck=163.34ns 1tp = 2ck, 1tl=296tp;
for serial output, input frequency = 12x3.061MHz, 1ck=27.23ns 1tp = 12ck, 1tl=296tp.



Edge coincidence for external SP and MCK is not necessary. EP is independent of MCK and SP

Figure 40. Differential input clock pulse

- **Input Timing**

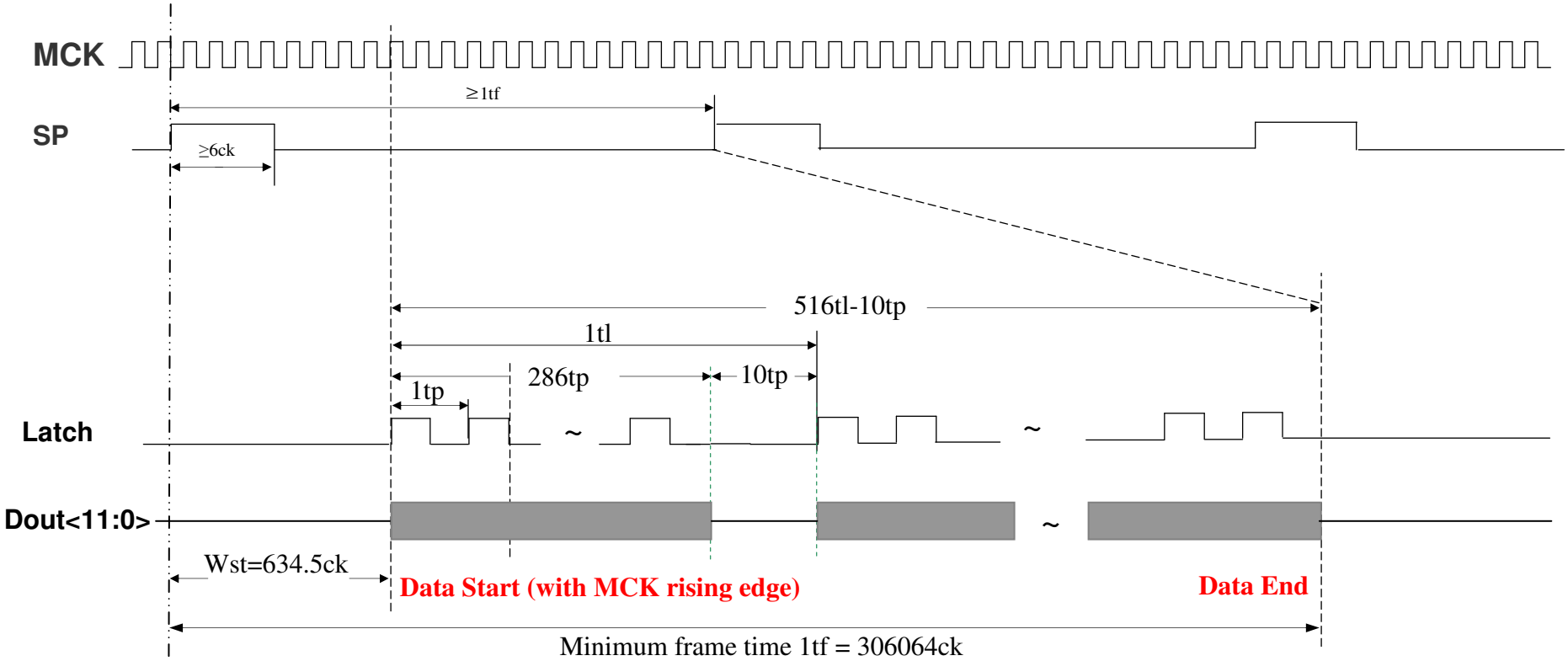


-SP(=SP+-SP-), MCK(=MCK+-MCK-), EP(=EP+-EP-) is output of LVDS_RX
- D_SEL, LSP, V_SEL, EN_DVC, HG and PWDN are 3.3V CMOS inputs and independent of SP, MCK
- Row wise gain control b<6:0> through I^2C

Figure 41. Relationship between input clock pulse and latch input control

■ Timing Diagram

- **Output Timing Diagram – Parallel**

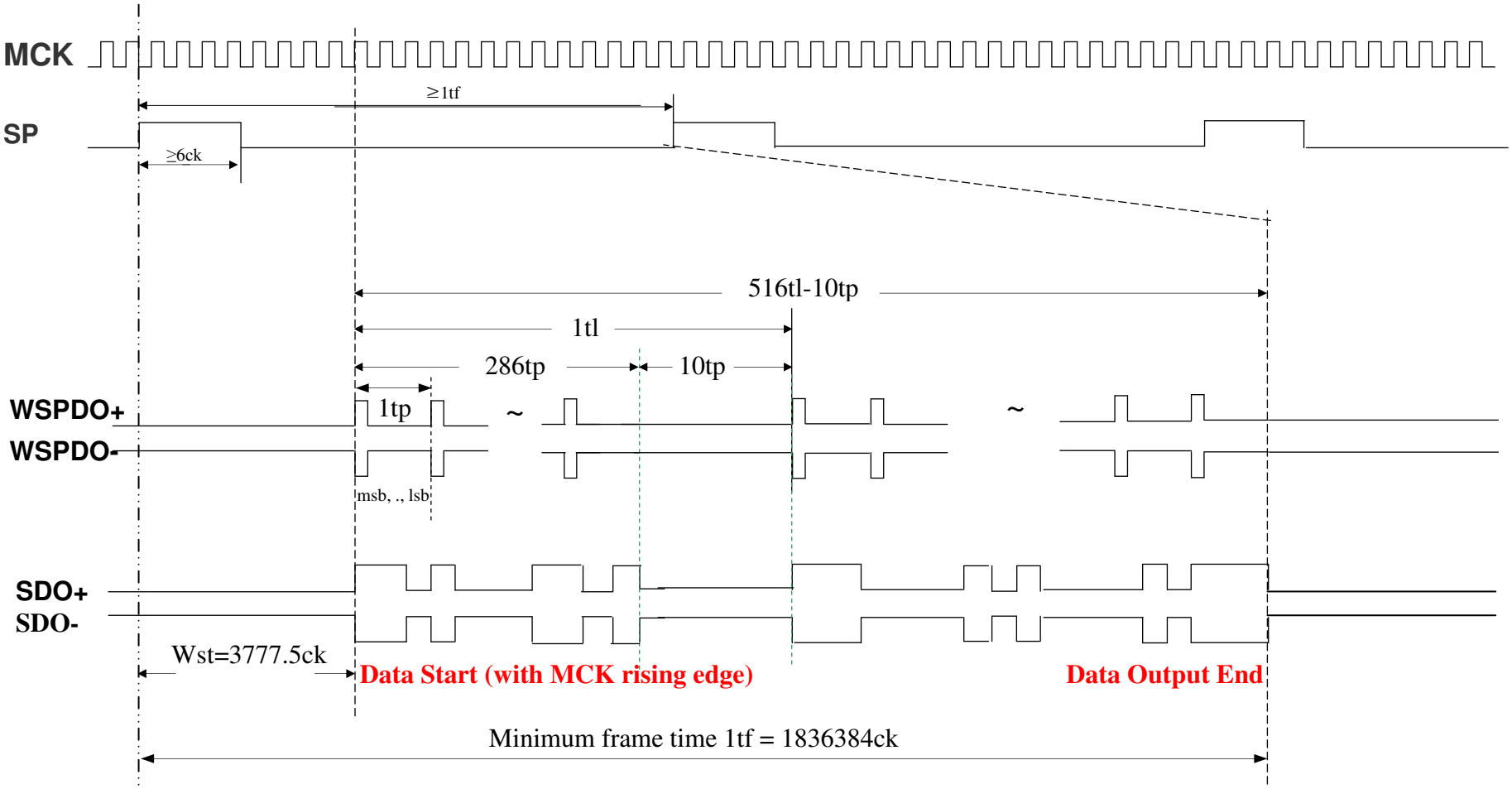


Wst = 8ck + 296x2ck (Transfer zone) + 10x2ck(Dump) +7.25tp (A/D latency) = 634.5ck
Minimum frame time = (634.5ck-8ck-7.25tp) + 516tl-10tp = 612ck + 516*296*2ck-10*2ck = 306064ck (153032tp)
(The ignored last dummy pixels eq to ADC latency)

Figure 42. Parallel data output timing diagram

■ Timing Diagram

• Output Timing Diagram – Series



Wst = 18ck + 296x12ck (Transfer zone) + 10x12ck(Dump)+87.5ck (A/D latency, p2s delay) = 3777.5ck
Minimum frame time = (3777.5ck-18ck-87.5ck) + 516tl-10tp = 3672ck + 516*296*12ck-10*12ck = 1836384ck (153032tp)

Figure 43. Serial data output timing diagram

CMOS Input / Output DC Electrical Characteristics

DC operating conditions (T = -15 C to 125 C)

Parameter	Symbol	Value			Units
		Min	Typ	Max	
Supply Voltage	VDD (Pin DVDD, VDD)	3.135	3.3	3.465	V
Active Supply Current	I_{VDD} I_{DVDD}			80 30	mA
Logic Hi	V_{IH}	0.7VDD		VDD+0.3	V
Logic Lo	V_{IL}	-0.3		0.3*VDD	V
Backup Reference Voltage	V_{REFP}		2.674		V

Table 5 DC operating conditions

CMOS Input / Output DC Electrical Characteristics

Input Pins: PWDN, HG, V_SEL, D_SEL, EN_DVC
(3.135 V < VDD < 3.465V, T = -15 ˚C to +125 ˚C)

	Symbol	Condition	Value			Units
			Min	Typ	Max	
High Level Input Voltage	V_{IH}		0.7*VDD		VDD+0.3	V
Low Level Input Voltage	V_{IL}		-0.3		0.3*VDD	V
High Level Input Current	I_{IH}	Input Buffer, Vin=VDD	-10		10	uA
Low Level Input Current	I_{IL}	Input Buffer, Vin=VSS	-10		10	uA
Switching Threshold	V_{OH}	At 3.3 V power supply		1.5		V
High Level Output Voltage	V_{OH}	At 1.6 mA load	0.7*VDD			V
Low Level Output Voltage	V_{OL}	At 1.6 mA load			0.5	V

Table 6 CMOS input / output electrical characteristics

LVDS TX and RX DC Electrical Characteristics

LVDS_TX

Output Pins: WSPDO±, SDO±
(3.135 V < VDD < 3.465V, T = -15 ˚C to +125 ˚C)

Parameter	Symbol	Conditions	Value			Units
			MIN	TYP	MAX	
Differential Voltage Swing	V_{OD}	RL=100 Ω	±300	±350	±400	mV
Change in Magnitude of V_{OD} for Complementary Output States	ΔV_{OD}				35	|mV|
Offset Voltage	V_{OS}		1.125	1.25	1.375	V
Change in Magnitude of V_{OS} for Complementary Output States	ΔV_{OS}				35	|mV|
Output High Voltage	V_{OH}				1.6	V
Output Low Voltage	I_{OL}		0.9			V
Output Driver Current	I_O		3.0	3.5	4.0	mA
Output Pins at Power Off	Z_O		High Impedance			

Table 7 LVDS DC electrical characteristics

LVDS_RX

Input Pins: CLK±, EP±, SP±
(3.0 V < VDD < 3.6 V, T = -15 ˚C to +125 ˚C)

Parameter	Symbol	Conditions	Value			Units
			MIN	TYP	MAX	
Differential Input High Threshold Voltage	V_{IH}	V_{CM}=1.25	-100			mV
Differential Input Low Threshold Voltage	V_{IL}				+100	mV
Common Mode Voltage Range	V_{CM}		0.6		2.3	V
Input Leakage Current	I_{LK}				20	uA

Table 8 LVDS RX electrical characteristics

6. DEVICE SPECIFICATION

6.1 Prime physical parameter specifications

6.1.1 Sensor chip

Item	Specification
Number of elements	256x512 active 20 dummy pixels shall be kept on active pixel number 1 side and 10 dummy pixels on active pixel number 256 sides. In addition 2 rows of dummy pixels at top and bottom.
Element Pitch	50 µm
Element size	50 µm x 50 µm (active area size)
No. of video ports	Single

6.2 Electrical and electro-optical parameter specifications

Item	Specification
Readout mode	Read while integrate Start and stop integration of all pixels should be simultaneous (snap shot)
Maximum Frame rate	2 x Fr or more
Minimum Frame rate	Fr / 5 or less
Dark Current	⩽ 9500 electrons/s/pixel for all pixels of the array
Noise floor in dark	⩽ 5 LSB
SNR:90% of Full well	⩾ 520
SNR: 50% of Full well	⩾ 360
SNR: 5% of Full well	⩾ 20
PSRR of the device	⩾ 60dB on all the supply lines at 2xFr readout frequency
Power consumption	⩽ 400 mW at 2x Fr readout frequency
Spectral response	
Full well capacity	⩾ 700Ke
Responsibility (for 12-bit quantization)	
Dark offset mean	⩽ 10 LSB at integration time Ti
Dark offset non-uniformity	⩽ 10 LSB RMS including FPN at integration time 10xTi
Along track MTF (516 row direction)	
Across track MTF (286 column direction)	
Residue (Line to Line)	⩽ 1% when alternate Lines are illuminated up to 90% of Full Well
Non-linearity at digital output	⩽ 1% in 10% to 90% of Full Well for any pixel ⩽ 2% outside this range

Missing Codes	Nil
Maximum non-uniformity	⩽ 2% RMS including FPN
Bad / defective pixels allowed	
Anti-blooming	

7. ABSOLUTE MAXIMUM RATINGS

Analog power supply voltage, VDD ---------- -0.3 to 4.0 V
Analog power supply current, I_{VDD} ---------- 100 mA
Digital power supply voltage, DVDD ---------- -0.3 to 4.0 V
Digital power supply current I_{DVDD} ---------- 40 mA
LVDS RX input voltage range ---------- -0.3 to VDD +0.3 V
CMOS Digital input voltage range, Vih ---------- -0.3 to VDD +0.3 V
Operating free-air temperature range, Ta ---------- -15 °C ~ 125 °C
Storage temperature range, Tstg ---------- -15 °C ~ 125 °C

≠ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8. RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Unit
Analog Power supply voltage	VDD	3.135	3.3	3.465	V
Analog Power supply current	I_{VDD}		80		mA
Digital power supply voltage	DVDD	3.135	3.3	3.465	V
Digital power supply current	I_{DVDD}		30		mA
LVDS RX common mode voltage	V_{CM}	0.6	1.25	2.3	V
LVDS RX differential voltage	Vdffin	V_{CM} –0.3		V_{CM} +0.4	V
CMOS High level input voltage	V_{ih}	VDD x 0.7		VDD+0.3	V
CMOS Low level input voltage	V_{iL}	0		VDD x 0.3	V
Clock frequency	f	0.1		6	MHz
Sensor integration time	t_{int}	20	50	250	ms
Wavelength of light source	λ	400		900	nm
Clock pulse high duty cycle		30		70	%
Operating free-air temperature	T_A	-15		125	°C

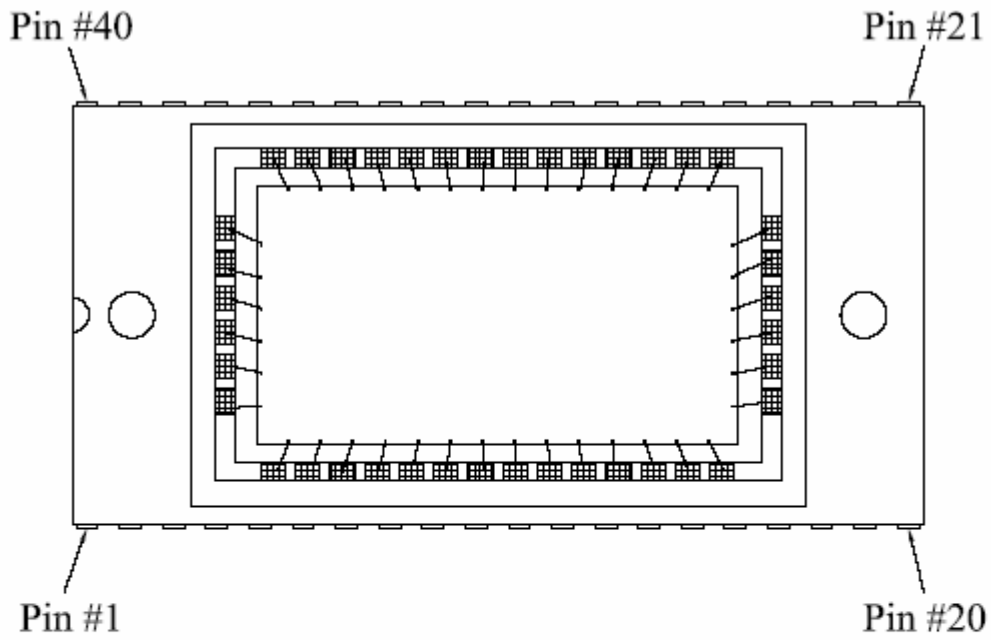
9. PIN DESCRIPTION AND PACKAGE

The following shows the pin description for C430.

Pin No	Pin Name	Type	Function description
1	AVDD	P	Analog power supply; 3.3 V
2	AVSS	P	Analog ground; 0 V
3	WSPDO-	LVDS-O	Word start output, LVDS (-)
4	WSPDO+	LVDS-O	Word start output, LVDS (+)
5	SDO+	LVDS-O	Video signal data output, LVDS (+)
6	SDO-	LVDS-O	Video signal data output, LVDS (-)
7	EP-	LVDS-I	Exposure control pulse input, LVDS (-)
8	EP+	LVDS-I	Exposure control pulse input, LVDS (+)
9	SP-	LVDS-I	Start pulse input, LVDS (-)
10	SP+	LVDS-I	Start pulse input, LVDS (+)
11	CP-	LVDS-I	Master clock input pulse, LVDS (-)
12	CP+	LVDS-I	Master clock input pulse, LVDS (+)
13	SDIO	DI/O	I2C input/output serial data
14	SCK	DI	I2C input clock
15	LSP	DI	Latch start pulse input
16	HG	DI	Coarse gain control, Lo: x2, Hi: x4
17	V_SEL	DI	External input voltage selection, Lo: disable, Hi: enable
18	D_SEL	DI	Parallel/Serial output data selection; Lo: Parallel output, Hi: Serial output
19	EN_DVC	DI	DVC selection; Lo: disable, Hi: enable
20	AVDD	P	Analog power supply; 3.3 V
21	DVDD	P	Digital power supply
22	DVSS	P	Digital ground
23	AVSS	P	Analog ground; 0 V
24	PWDN	DO	Power down
25	DOUT<0>	DO	ADC output, LSB
26	DOUT<1>	DO	ADC output
27	DOUT<2>	DO	ADC output
28	DOUT<3>	DO	ADC output

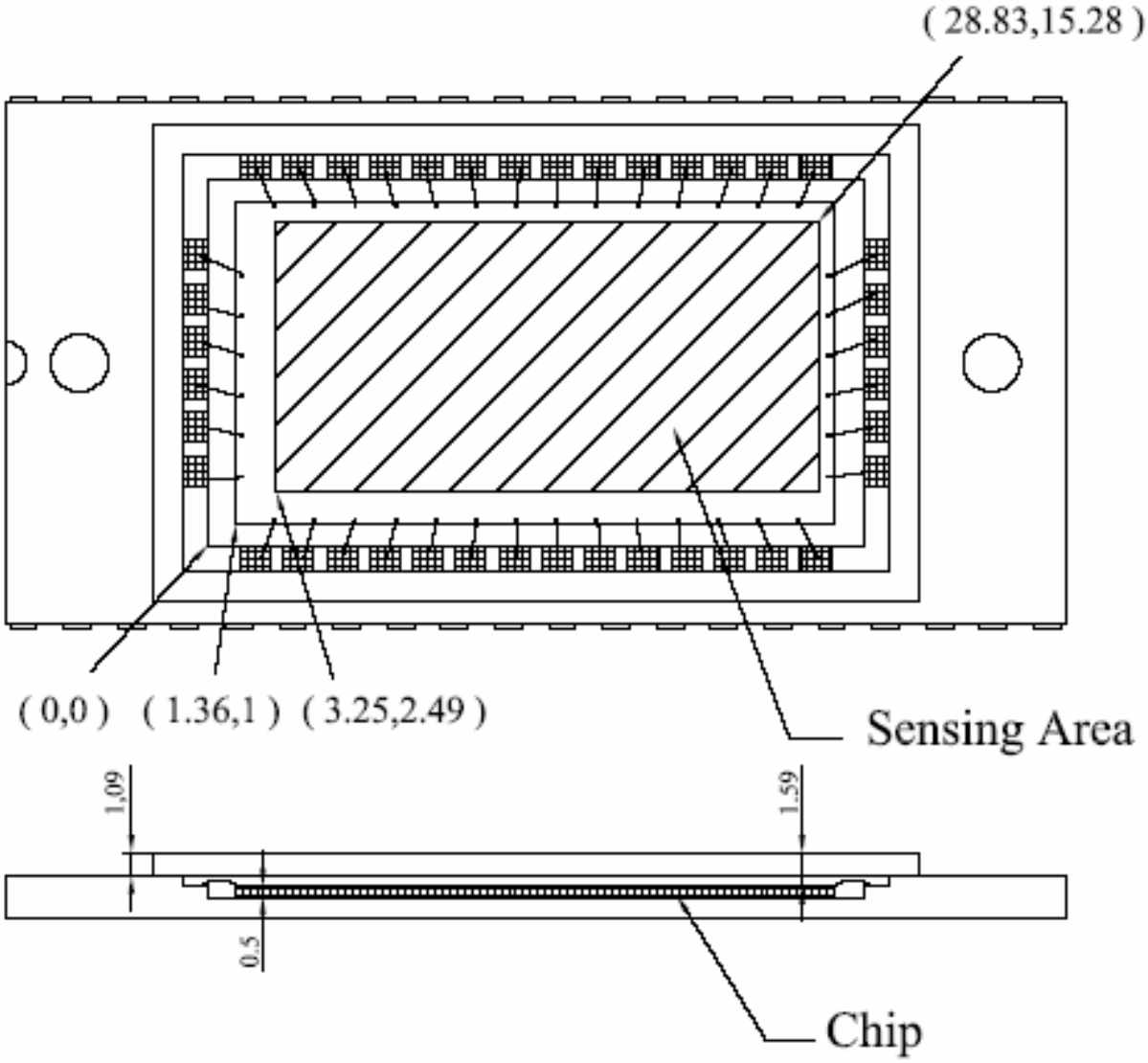
29	DOUT<4>	DO	ADC output
30	DOUT<5>	DO	ADC output
31	DOUT<6>	DO	ADC output
32	DOUT<7>	DO	ADC output
33	DOUT<8>	DO	ADC output
34	DOUT<9>	DO	ADC output
35	DOUT<10>	DO	ADC output
36	DOUT<11>	DO	ADC output, MSB
37	Latch	DO	ADC output data latch pulse
38	VI	AI	External input voltage
39	RREF	AO	Reference voltage output
40	DVSS	P	Digital ground

■ Pin Diagram



Pin	Name	Pin	Name	Pin	Name	Pin	Name
01	AVdd	11	cp-	21	DVdd	31	dout<6>
02	AVss	12	cp+	22	DVss	32	dout<7>
03	WSpdo-	13	sdio	23	AVss	33	dout<8>
04	WSpdo+	14	SCK	24	pwdn	34	dout<9>
05	Sdo+	15	Lsp	25	dout<0>	35	dout<10>
06	Sdo-	16	hg	26	dout<1>	36	dout<11>
07	ep-	17	V_sel	27	dout<2>	37	Latch
08	ep+	18	d_sel	28	dout<3>	38	Vi
09	sp-	19	en_dvc	29	dout<4>	39	refp
10	sp+	20	AVdd	30	dout<5>	40	DVss

■ Chip Location (unit: mm)



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