March 2008

C640

4000 ELEMENTS LINEAR IMAGE SENSOR

DATA SHEET

Contents

1. GENERAL DESCRIPTION

The C640, 4000 elements linear image sensor is designed to provide high resolution, low power consumption for machine vision and spectroscopy applications. The C640 is a mixed mode silicon on chip (SOC) IC. It combines analog circuitry, digital circuitry and optical sensor circuitry all on one chip. This chip integrates active pixel sensor array, programmable gain amplifier (PGA), 12 bit analog to digital converter (ADC), voltage regulator, low voltage differential amplifier (LVDS) and timing generator together. These image processing functions including Coarse gain control and Fine gain control can be latched through external latch start pulse.

The device can operate in Single Frame Pixel Charge Capture mode, Multi-frame Pixel Charge Accumulation mode or Power down mode:

-Single Frame Pixel Charge Capture mode, each pixel of the signal is readout and then reset for each frame.

-Multi-frame Pixel Charge Accumulation mode, each pixel of the signal is not reset during readout. The video signal of each pixel is accumulated during next frame. The second frame pixel charge adds to (accumulates) the charge of first frame pixel charge. The Multi-Frame Accumulation mode can accumulate up to thirty-two (32) frames. Therefore, the video signal of each individual pixel can be integrated up to thirty-two (32) frames compared to the single capture in one (1) frame. This unique function enables the device to be suitable for extremely low light level application.

-Power down mode, all of the blocks are power down except latch block to save power.

This device uses CMOS Sensor's proprietary advanced APS technology and readout structure to reduce the fixed pattern noise, increase dynamic range and improve linearity. The device consists of 4000 photodiode elements. The pixel size is 7 um square on an element pitch of 7 um.

2. FEATURES

- 7 um x 7 um pixel size
- 7 um element pitch
- 4000 active elements and 30 dummy elements (20 dummy at starting and 10 dummy at end for dark signal cancellation)
- 28000 um x 7 um image size
- Single video readout, 12 bit resolution, serial readout mode

- Three operational modes: Single Frame Pixel Charge Capture, Multi-Frame Pixel Charge Accumulation, and Power Down
- Snap Shot Operation (start and stop integration for all pixels simultaneously)
- Auto dark voltage cancellation and fixed pattern noise cancellation
- Programmable gain control feature:
  - Two bits for Coarse gain of (x1, x2, x3, and x4)
  - Three bits for Fine gain of ± 10%
- Global exposure control function (no integration will take place till exposure control is active)
- ADC input selects either internal PGA output or external input voltage to connect to ADC input
- Externally controlled independent pins to set the device for gain, ADC input selection, dark voltage cancellation selection, operational mode (Single Frame Capture / Multi-Frame Accumulation) and Power Down mode. All input setting pins are provided in CMOS interface. The gain setting pin is latched by an external latch start pulse (LSP)
- Electronic Shutter is controlled by Exposure Pulse (EP)

3. APPLICATIONS

- Machine Vision, Spectroscopy

4. DEVICE DESCRIPTION

4.1 System Overview

Figure 1 shows a functional block diagram of the C640 active pixel sensor. It includes the following functions

- 4000 active pixels and 20 dummy pixels on active pixel number 1 side and 10 dummy pixels on active pixel number 4000 side
- Fixed pattern suppression circuitry
- Dark voltage cancellation circuitry
- Programmable gain amplifier (PGA) for coarse and fine gain control
- 12 bit analog to digital converter (ADC)
- Global exposure control circuitry
- Timing generator to generate internal clock
- Power down mode through external command
- Low voltage differential signal (LVDS) driver / receiver for clocks and output data line

(Note: Output data line cable can be up to 0.5Meter; Longer length possible but not tested)

- Data format for ADC data output serialization
- Band gap and voltage regulator for referencing ADC and PGA
- Divided by 12 counter for internal timing generator from external clock
- Single end to dual voltage converter

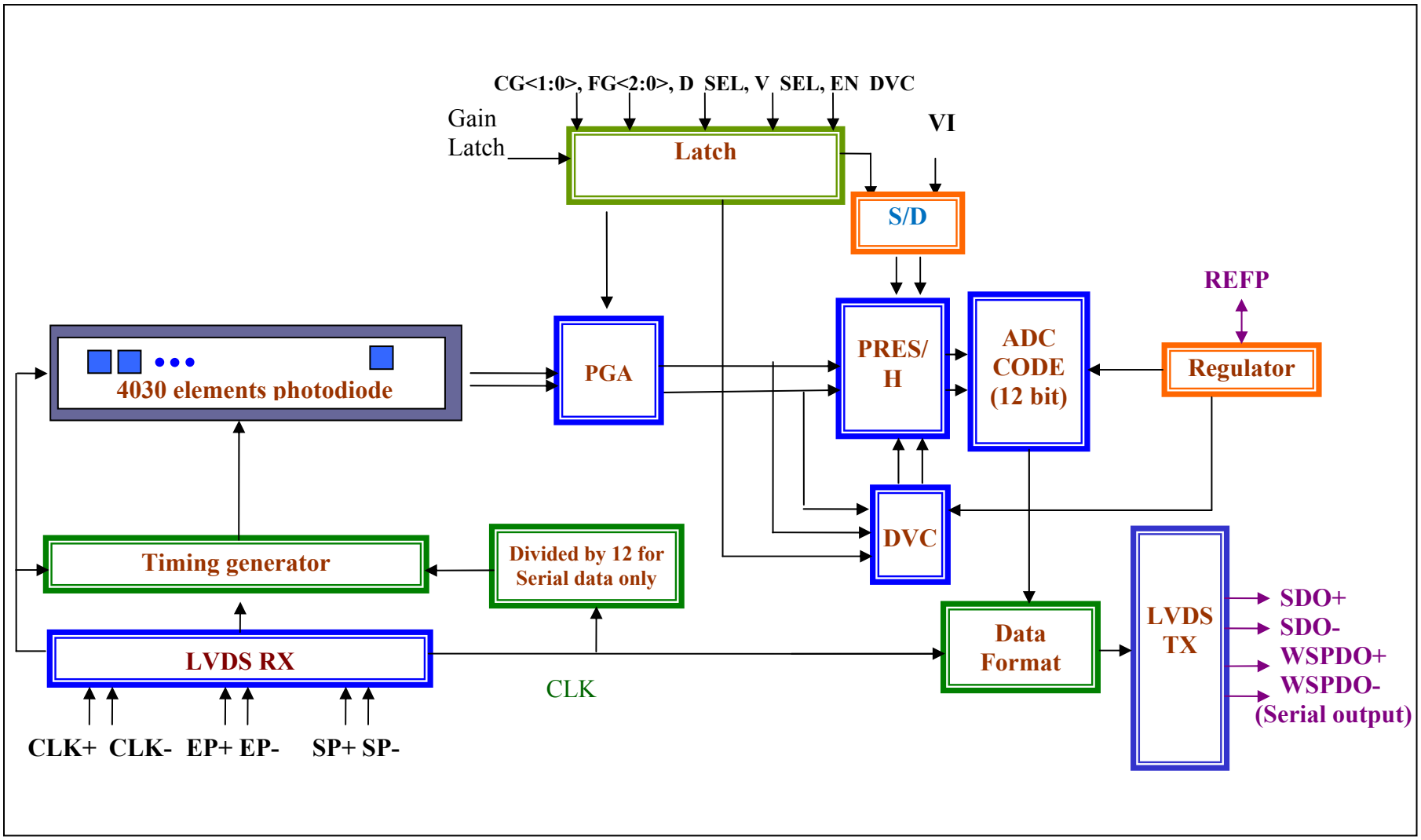


Figure 1. The block diagram of the C640 sensor chip

Based on the device function, the C640 device is separated into (1) sensor stage, (2) gain control stage, (3) ADC and reference voltage stage, and (4) input / output control stage. The functionality of each stage is explained as follows.

4.2 Sensor stage

There are a total of 1 x 4030 elements. CMOS Sensor's proprietary advanced active pixel sensor (APS) readout structure is used to convert the charge which accumulates on the photo detector into a voltage signal. This technology provides both a fixed pattern noise (FPN) suppression functionality and improves the uniformity of the pixel array. CMOS Sensor's proprietary Buffer Mux technology is also used to readout each pixel signal at each clock rate. The Buffer Mux circuitry also performs as a Coarse gain control. Resulting from a switch capacitor method being used to build the Buffer Mux, the linearity is further improved and the fixed pattern noise is further reduced.

4.2.1 Image Sensor Array

A total of 4000 active pixels are designed on this array. Each element pitch is 7 um thus forming a full sensor length of 28 mm. For each photodiode element, the light sensing area is a 7 um by 7 um rectangular region defined by an aperture in an opaque mask. Rectangular shaped photodiodes extend across the aperture and are connected to the storage capacitor that is buried under the mask. This technique is used to adjust the full well capacity of each pixel. The entire aperture is photosensitive such that photocurrent generated by light incident between the photodiodes will be collected by the nearest diode. Figure 2 shows the aperture geometry showing the idealized response function that would be obtained by scanning a point source of visible light along the length of the aperture.

As shown in Figure 2, the dimension of the aperture width of "c" is 7 um, the pixel pitch "b" is 7 um and the photodiode width "a" is 5 um.

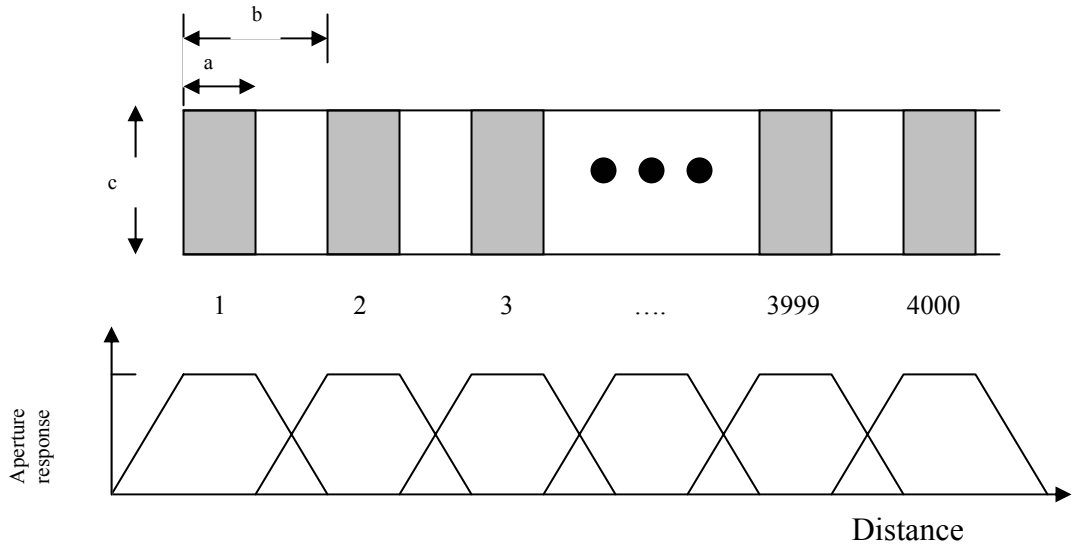


Figure 2. Sensor geometry and idealized aperture response

In additional to the active pixel, optical black (OB) pixels are designed to provide a dark reference voltage and eliminate edge effect. The optical black pixels are arranged for 20 pixels on the beginning of 1st active pixel and 10 pixels after the 4000th active pixels. Therefore, the total number of the image sensor equals to 4030 pixels. The optical black pixels are the same as active image sensor except they are covered by a light shielding opaque element. Figure 3 shows the pixel arrangement of the sensor array.

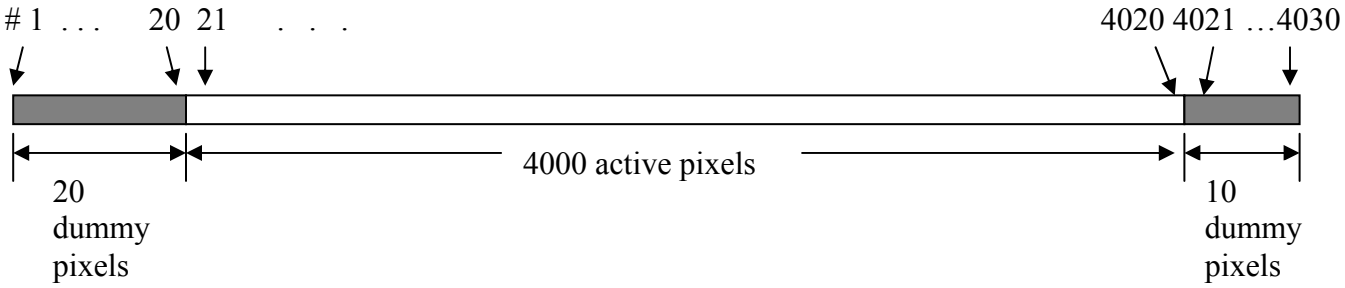


Figure 3. The pixel arrangement of the sensor array

4.2.2. Multi-Frame Pixel Charge Accumulation Mode

C640 allows external control of video signal pixel charge accumulation across multiple frames.

Frame integration count from 2 to 32 frames is controlled by pins D_Sel, and EP. Multi-Frame Accumulation mode is enabled when D_Sel is High. Pixel charge is accumulating frame to frame when EP is High. Pixel Reset occurs when SP goes High to Low when EP is Low shown on

Figure 19: Timing Diagram of the Multi-Frame Pixel Charge Accumulation Mode. .

4.2.3. Advanced Charge trans-impedance amplifier (CTIA) readout structure

C640 sensor utilizes CMOS Sensor's proprietary advanced Charge trans-impedance amplifier technology. This structure utilizes a charge integrator that provides linearity throughout the full dynamic range. In addition, there is a significant increase in immunity from the power supply and ground noise as compared to the conventional APS circuitry. The gain of the advanced CTIA readout structure is higher than the conventional APS technology described below and the reset noise is eliminated. The non-linearity is less than 0.05% on the whole video output range.

Figure 4 shows a conventional APS structure. It consists of a photodiode, a reset transistor, a source follower, and a readout switch. When readout switch is turned on, the photodiode voltage will be readout by the source follower. There are, however, several drawbacks on this conventional circuitry approach. The gain of the source follower is always lower than 1 and is non-linear. In addition, the power supply and ground noise are very difficult to prevent on this structure.

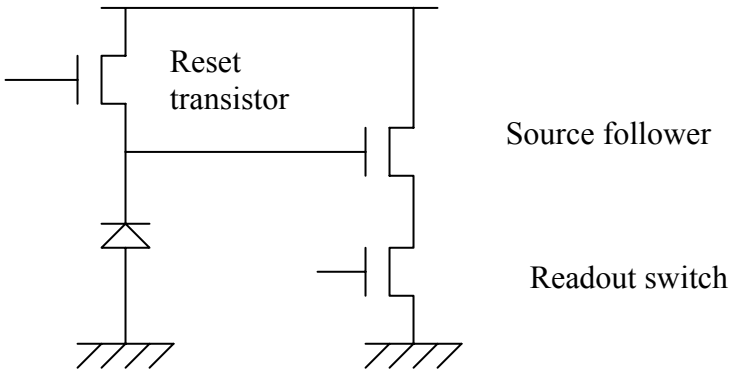


Figure 4. Schematic of conventional APS circuitry

4.3 Gain control stage

Figure 5 shows the block diagram of the gain control stage. It consists of Buffer Mux & Coarse gain control block, PGA, Fine gain control block, Dark Voltage Cancellation (DVC) block, and Subtract (x2) block. Two sets of gain control are used to adjust the global gain of the device. One is Coarse gain control and the other is Fine gain control. Two bit (CG<0> and CG<1>) of the input pin is used to control the Coarse gain of x1, x2, x3, and x4. Three bit (FG<0>, FG<1> and FG<2>) of the input pin is used to adjust the Fine gain of ± 10% based on the Coarse gain. This device has an option to select either dark voltage cancellation or without dark voltage cancellation. The functionality of each block is explained as follows.

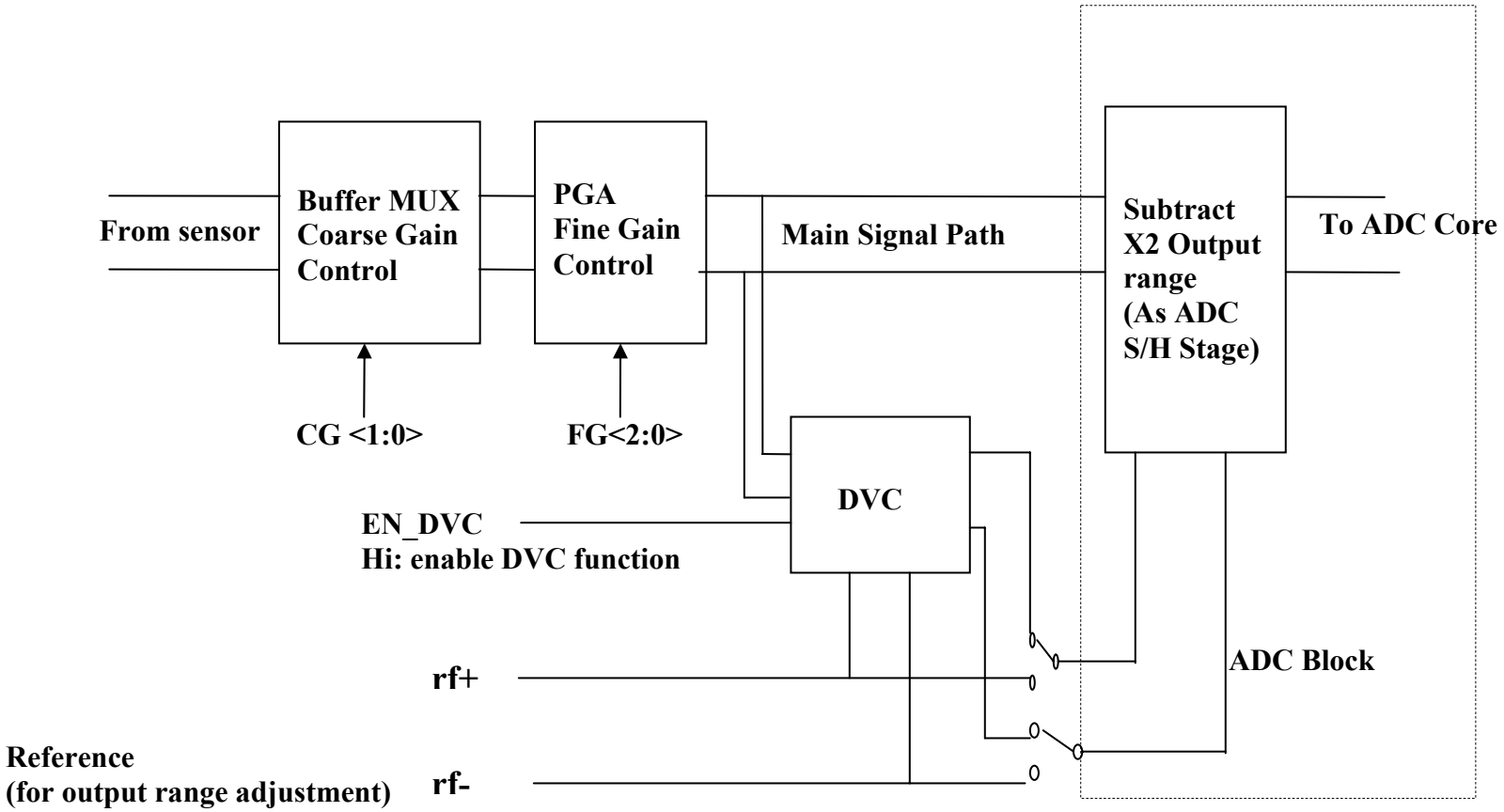


Figure 5. Gain control stage of the C640 sensor

4.3.1 Buffer mux and Coarse gain control

For this Buffer Mux design, we use a charge integrator to convert the pixel signal. Since all of the signals go through this single charge integrator, the fixed pattern noise is eliminated. In addition, the amplifier on the charge integrator utilizes a dual differential amplifier to eliminate both power supply noise and ground noise.

The Coarse gain can be adjusted to x1, x2, x3 and x4. Two control bits (CG<0>0 and CG<1>) are used to adjust the output amplifier gain. The Coarse gain control table is shown in Table 1. Figure 6 shows the linearity characteristics for four different Coarse gains. The non-linearity is less than 0.02% for the whole voltage range.

In conventional CDS circuitry, each pixel of a conventional readout structure uses two source follower amplifiers. There are several drawbacks to such a source follower approach. Wafer process variation causes a variation in the gain and offset for each source follower resulting in a significant fixed pattern noise problem. In addition, the gain of the source follower is less than one.

4.3.2 Programmable Gain Amplifier (PGA)

The output signal from Buffer Mux is connected to the programmable gain amplifier (PGA) which allows adjustment with the Fine gain. Fine gain variation of ±10% on Coarse gain value is controlled by three external pins FG<2:0>. A switch capacitance technique is used on the PGA block. Three bit of the external input pin is used to adjust the fine gain value. The Fine gain control table is explained on Table 2 and the simulated linearity characteristics of the Fine gain presented in Figure 7. The non-linearity is less than 0.1%.

4.3.3 Dark voltage cancellation circuitry

The charge (Q_d) generated from dark current on the opaque pixel is shown as follows:

$$Q_d = I_d * T_{int}$$

Where I_d is the dark leakage current on the opaque pixel,

T_{int} is the integration time.

The charge (Q) generated from active pixel is shown as:

$$Q = (I_L + I_d) * T_{int}$$

Where I_L is a light current generated from incident light.

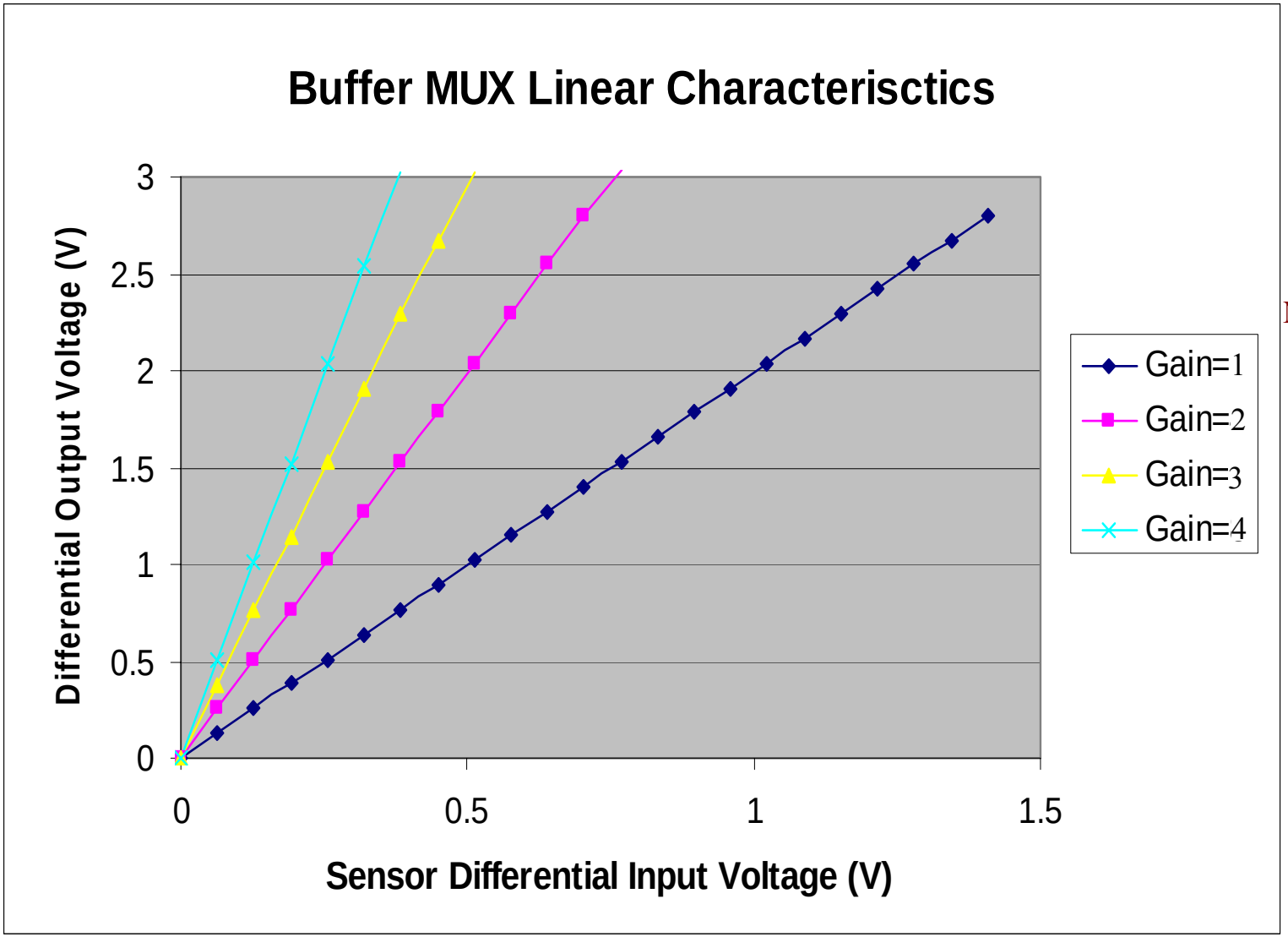
I_d is the dark leakage current on the active pixel.

The dark voltage on the opaque pixel is the same as active pixel. By clamping the DC voltage on the opaque pixel, the dark leakage current is subtracted. The output video signal from the dark voltage cancellation circuitry is the real video signal that is generated from incident light.

Coarse Gain is controlled by Two external Pins CG<1:0>

Gain	CG<1>	CG<0>
X 1	0	0
X 2	0	1
X 3	1	0
X 4	1	1

Table 1 Coarse gain control table.



Non-linearity:

< 0.02%
< 0.02%
< 0.02%
< 0.01%

Figure 6. The linearity property of the coarse gain

Fine Gain Control

Fine Gain Setting: FG<2:0>

Gain	FG<2>	FG<1>	FG<0>
-10%	0	0	0
-7.14%	0	0	1
-4.28%	0	1	0
-1.42%	0	1	1
+1.42%	1	0	0
+4.28%	1	0	1
+7.14%	1	1	0
+10%	1	1	1

Table 2. Fine gain table on the C640 device

Fine gain control Linearity (non-linearity < 0.1%)

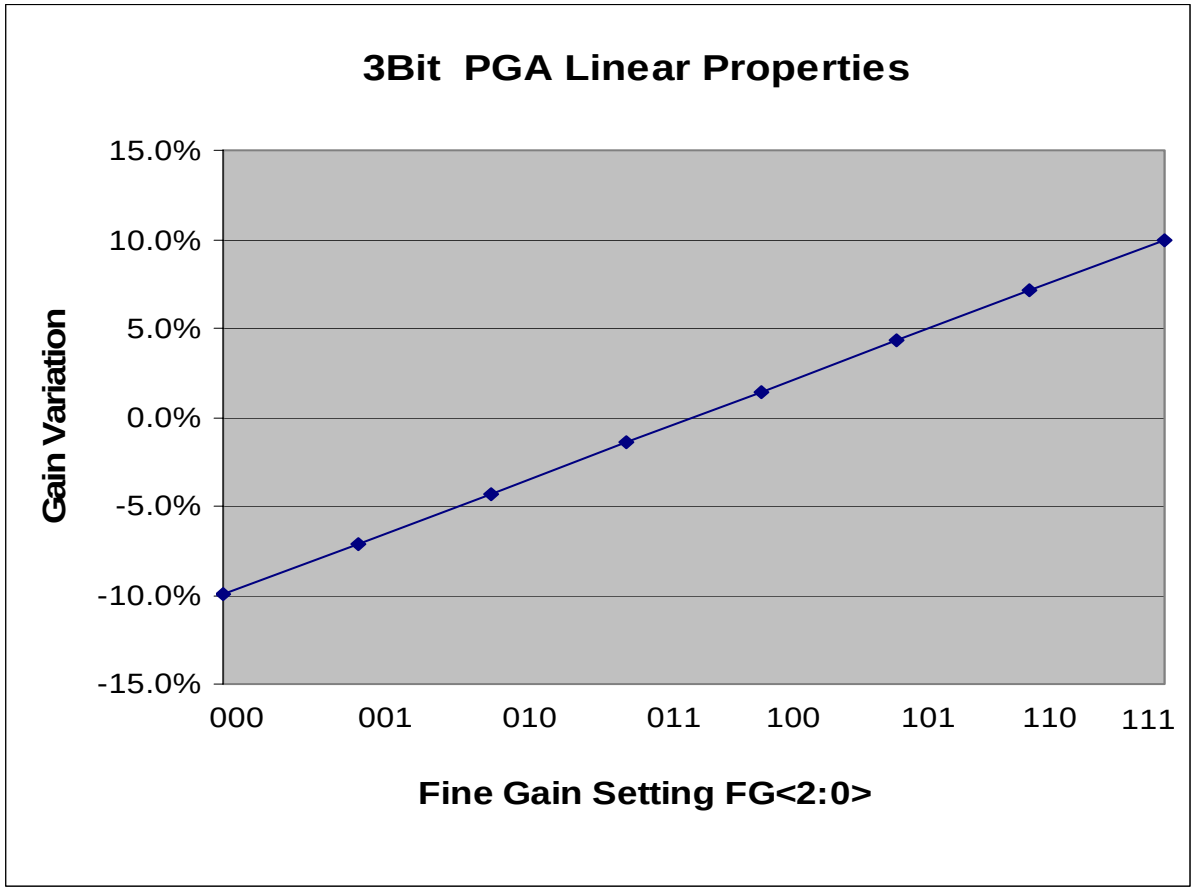


Figure 7. Linear characteristics of the three bit Fine gain

4.4 Analog to Digital Converter (ADC) and reference voltage generator

A 12 bit pipeline Analog to Digital Converter (ADC) is used to convert from analog signal to digital number (DN). Figure 8 shows the block diagram of the 12 bit ADC and reference voltage. A pipeline ADC structure is used for the 12 bit ADC design since it has high speed and high performance characteristics.

The band gap and reference voltage block support the reference voltage of the ADC block. This reference voltage provides a very stable voltage to the ADC. When either temperature or the power supply voltage is changed, the reference voltage is still kept constant. The reference voltage of the ADC is normally adjusted to maximum 2.048 V. This value represents the full scale of the ADC input range.

Customer Test Option: In order to test the performance of the ADC, an external VI, bonding pad and a multiplexing switch is used. An input saw-tooth waveform is then applied to the ADC. By comparing the waveform of the analog input and digital number (DN), any missing code after the ADC can be detected. In the normal operation mode, the output from PGA is connected to the input of the ADC.

4.4.1 12-bit ADC

Figure 9 shows a system block diagram of the 12-bit ADC converter. It consists of (1) a pre sample / hold, (2) a 12-bit pipeline ADC core and (3) a digital correction output buffer. The 12-bit pipeline conversion core consists of 11 conversion 1.5-bit stages and 1 conversion 1-bit stage. There is a total of 23 bit of the digital output from 12-bit conversion core. The pipeline ADC achieves high speed, high performance and low noise for this application.

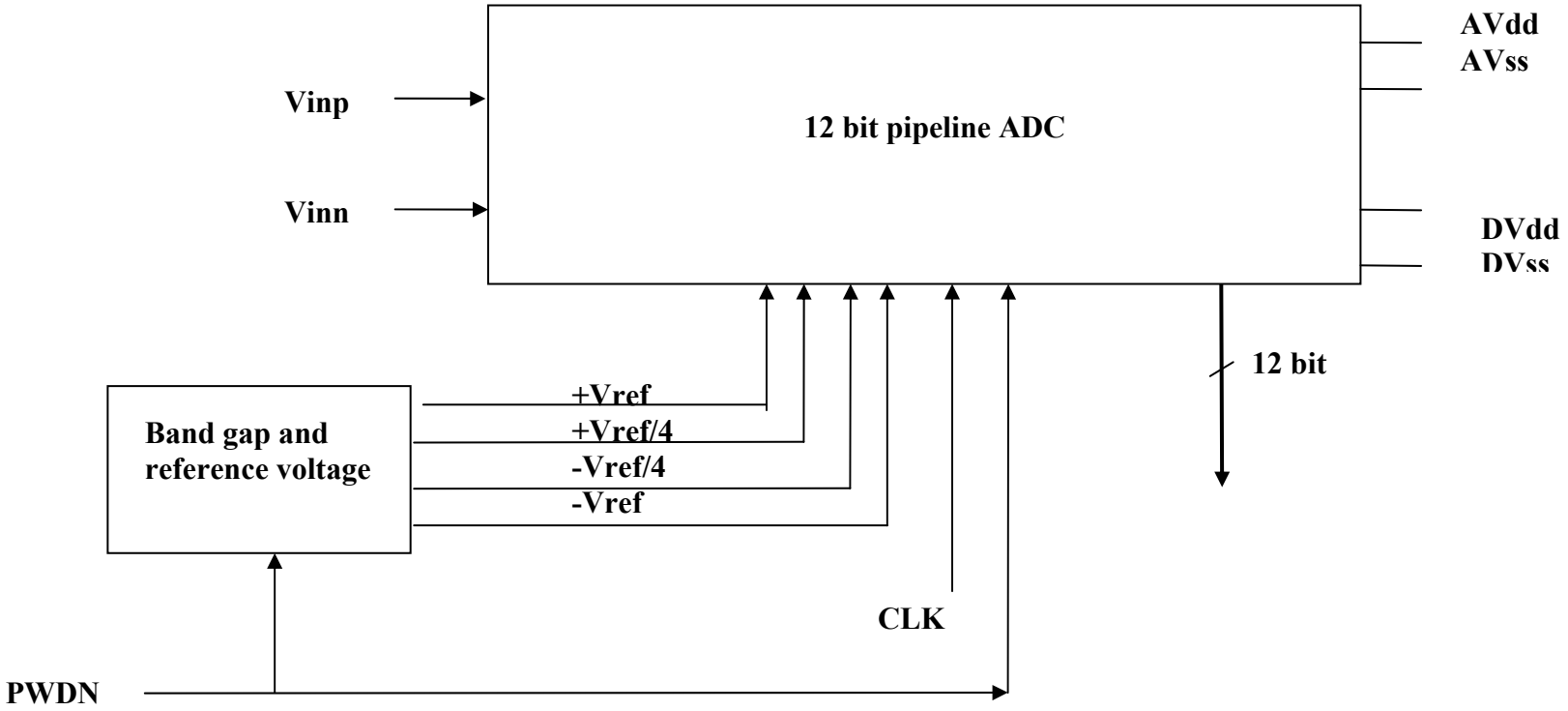


Figure 8. Block diagram of the 12 bit ADC and reference voltage

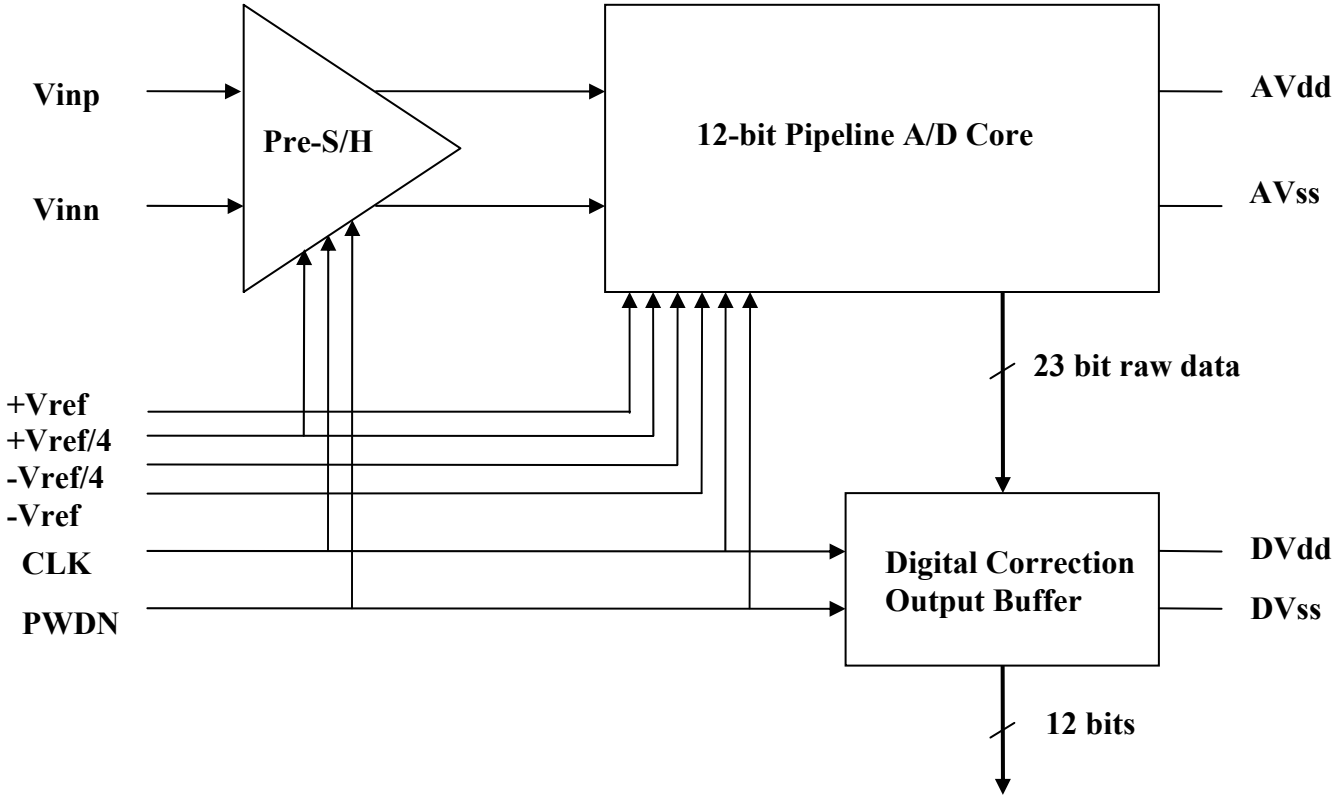


Figure 9: 12 Bit A/D Converter ADC

4.5 Input and output stage

This stage consists of (1) data input control, (2) data output control, and (3) external analog input voltage control. The functionality of each control will be explained in the following.

4.5.1 Data input control

Figure 10 shows the block diagram of the data input control. It consists of (1) LVDS receiver block, (2) latch block, (3) Timing generator and divided by 12 blocks. All of the timing to operate the device is generated from divided by 12 and timing generator block.

4.5.1.1 Divided by 12 counter

The input master clock (CLK) and external start pulse (SP) go thru a "divided by 12 counter" block and generated pixel clock pulse and initiated start pulse. The master clock is also used for the clock frequency on the parallel to serial converter (Figure 10: Data Input Control). Input Master Clock (CLK) goes thru LVDS where internal master clock (MCK) and internal StartPulse (SP) are provided to the Timing generator block (Figure 10: Data Input Control).

4.5.1.2 Timing Generator

Only three input clock pins are required for this device. One is master clock (CLK about 30 MHz); second is a synchronized clock pulse (SP) and third is exposure control pulse (EP). The timing generator block provides the logic circuitry to operate this device and it controls the following functions.

- Image sensor array control and three different modes of operation

  (Single Frame Capture, Multi-Frame Accumulation and Power Down)
- Provide the timing for the readout circuitry
- Provide the timing for Auto exposure control, dark voltage cancellation, and gain control
- Provide the timing for ADC and data format
- External output timing (SDO and WSPDO)

4.5.1.3 LVDS Receiver block

The differential LVDS input clock pulse converts from differential input pulse to the CMOS clock pulse. Three input clock pulses (CLK, SP and EP) are applied to the device. These three input clock

pulses connect to the divided by 12 block and timing generator block and generate all necessary clock pulses to operate sensor, gain stage and ADC.

4.5.1.4 Power on default setting

All default digital settings except PWDN is loaded by the power ON reset circuitry (POR) as shown in Table 3. The PWDN is independently controlled by the digital settings at the PWDN pin (imaging mode PWDN=0 (default) and power down mode PWDN=1).

Coarse gain CG<1:0> and Fine gain FG<2:0> is loaded by the LSP (width > 5 clock cycle). The EN_DVC, D_SEL and V_SEL are loaded at the start of every frame.

Input pin name	Default Value	Description
CG＜1:0>	00	Coarse gain = 1
FG<2:0>	000	Fine gain = 0.9
V_SEL	0	Select input voltage to the ADC 0 = image sensor; 1 = External input pin, VI
D_SEL	0	Select Single Frame or Multi-Frame mode 0 = Single Frame Capture ; 1 = Multi-Frame Accumulate
EN_DVC	0	Enable dark voltage cancellation circuitry 0 = Disable; 1=Enable

Table 3. Power on default setting value of the C640 device

4.5.2 Data output control

Figure 11 shows the block diagram of the data output control. It consists of (1) data format block, and (2) LVDS transmitter block. The data format is a parallel to serial converter. It converts 12-bit

parallel data output from ADC block to a serial data output. This data then goes thru the LVDS transmitter to convert to the LVDS differential clock pulse.

4.5.2.1 LVDS Transmitter (TX) block

The single end CMOS input clock pulse converts to the differential clock pulse. There are two clocks pulse data outputs (SDO and WSPDO). The SDO is a serial data output; and the WSPDO is a word start pulse for each data output. The output data cable length can be up to 0.5Meter in length. Longer lengths are possible but not tested by CMOS Sensor.

4.5.3 External input voltage control

Customer Test Option: In order to test the ADC performance, an external input voltage control is applied to the ADC. Figure 12 shows the block diagram of the external input voltage control. It consists of one single end to differential converter. When V_SEL is low, the ADC input is connected to the gain control stage. The video signal is an image sensor video signal. When V_SEL is high, the ADC input is connected to the external input voltage, VI.

Data input control block diagram

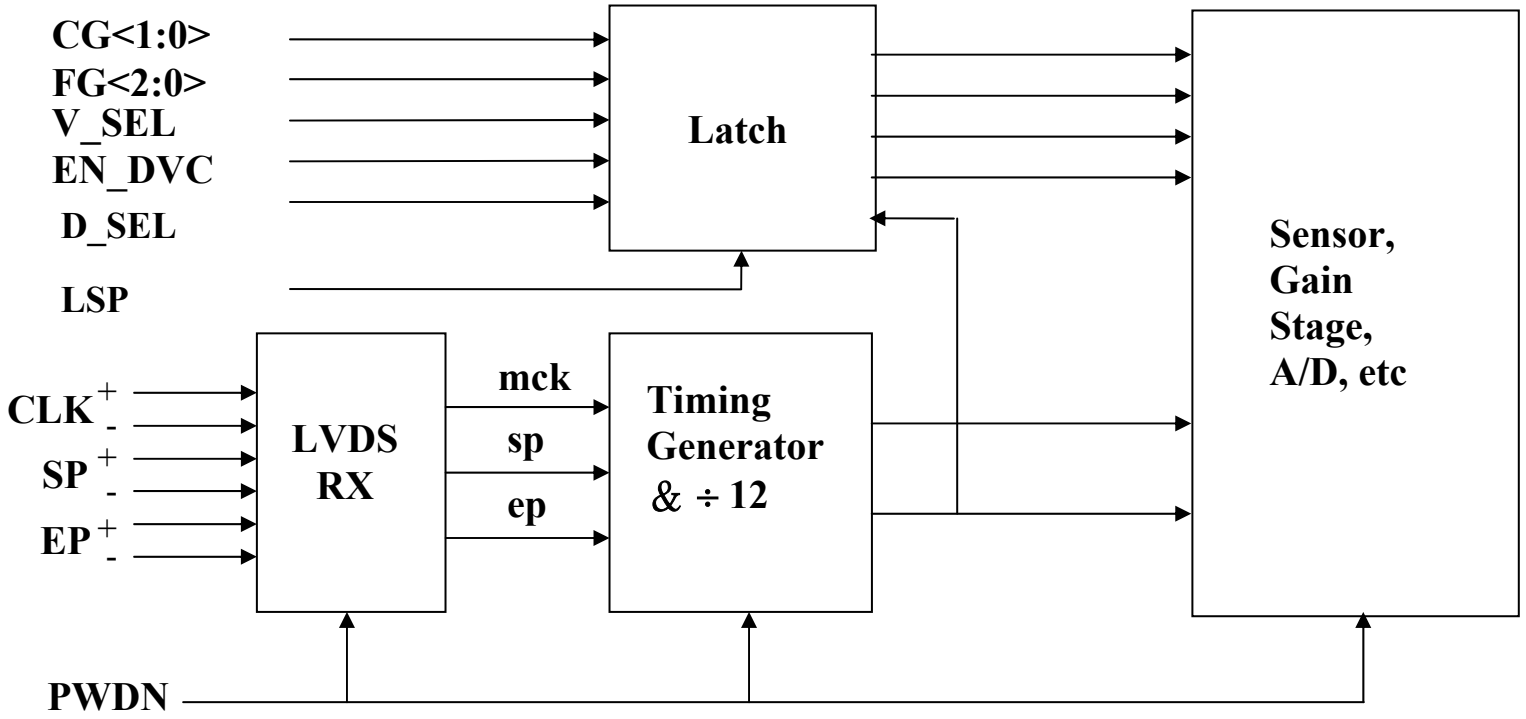


Figure 10: Data Input Control

Data output control block diagram

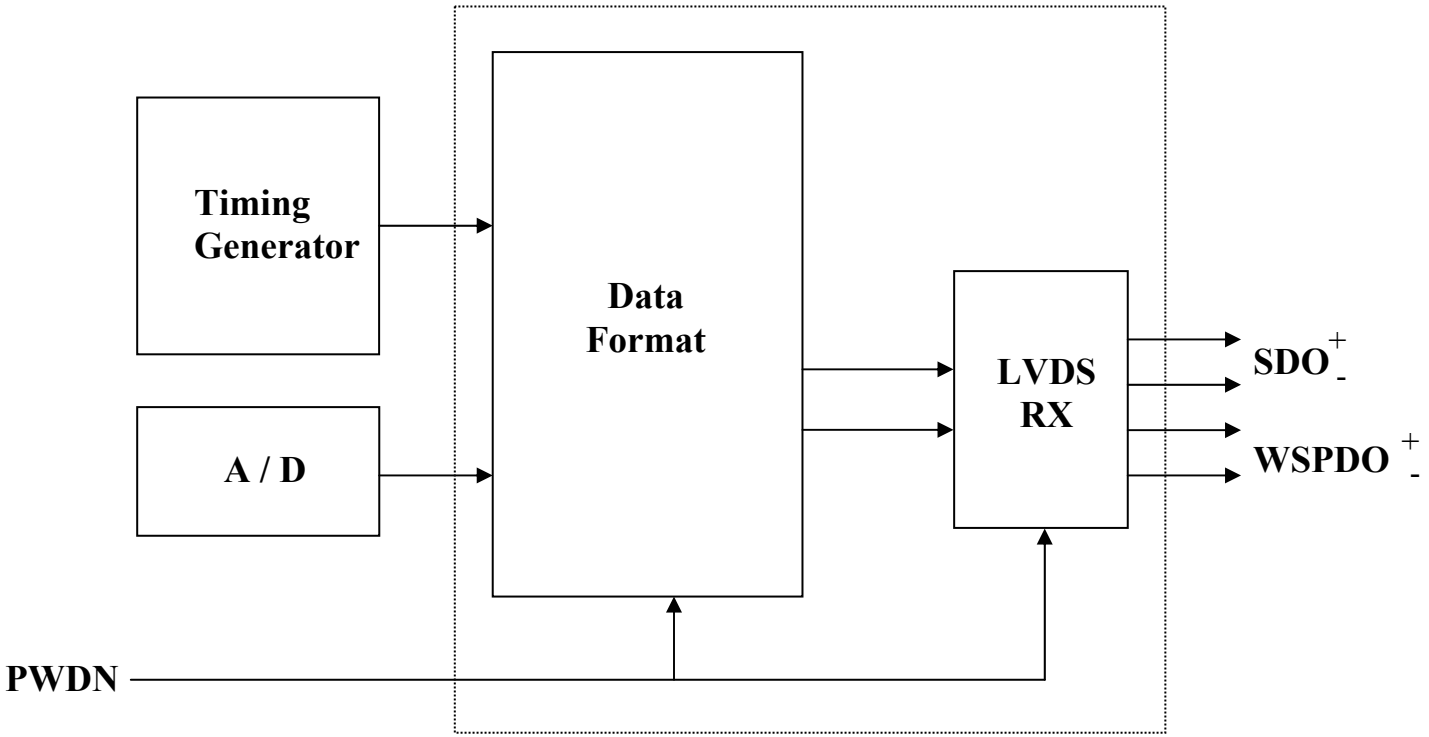


Figure 11. Block diagram of the Data output control

External input voltage control

V_SEL Hi: ADC input from external input pin, VI.
Lo: ADC input from image sensor

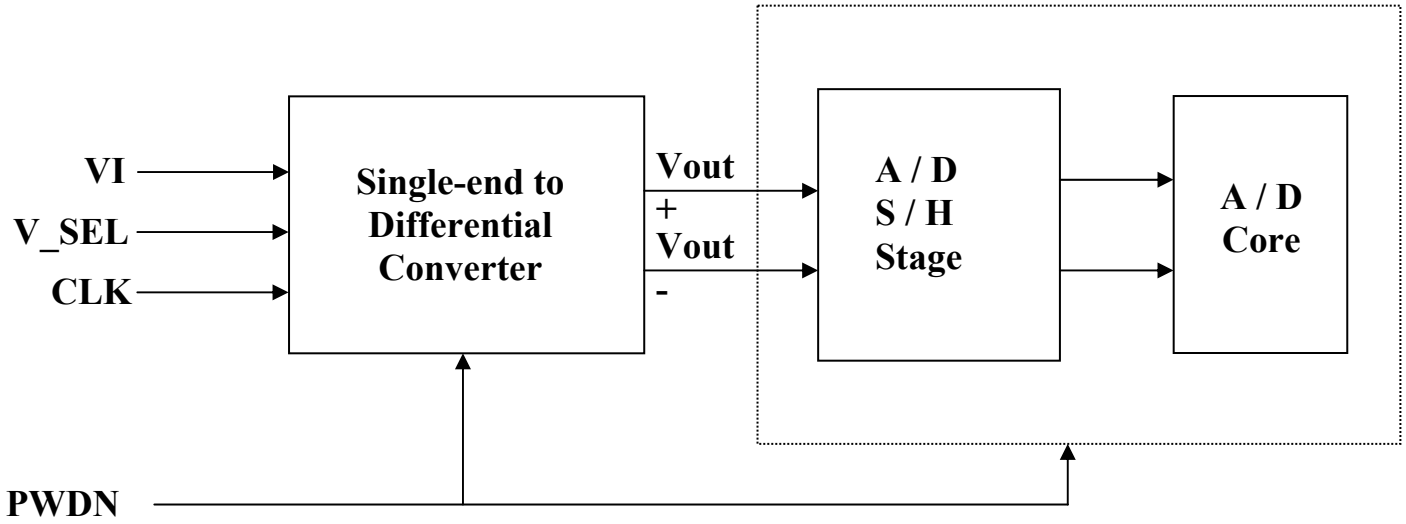


Figure 12. Block diagram of the external input voltage control

5. ELECTRIC CONFIGURATION AND EXTERNAL INTERFACE

External Interface

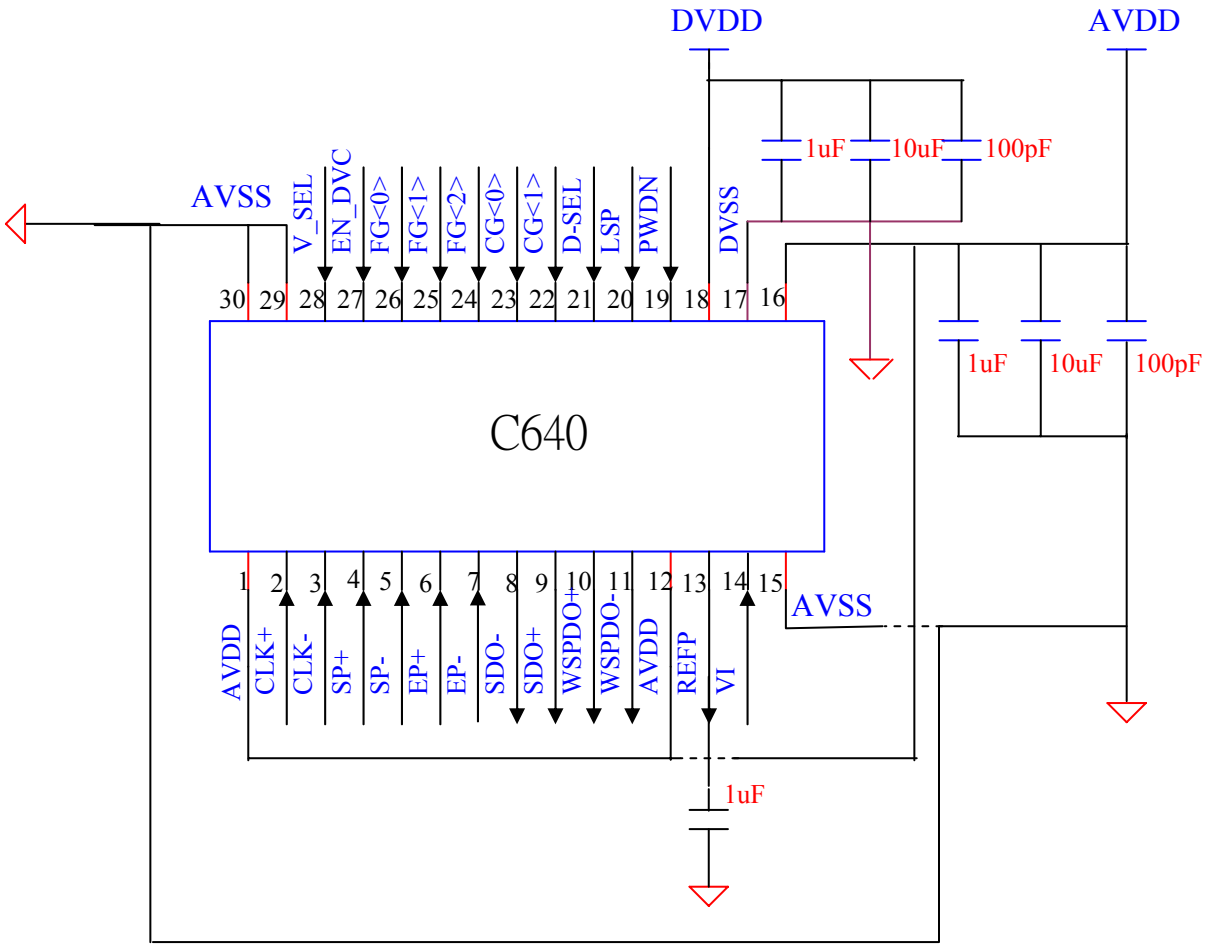
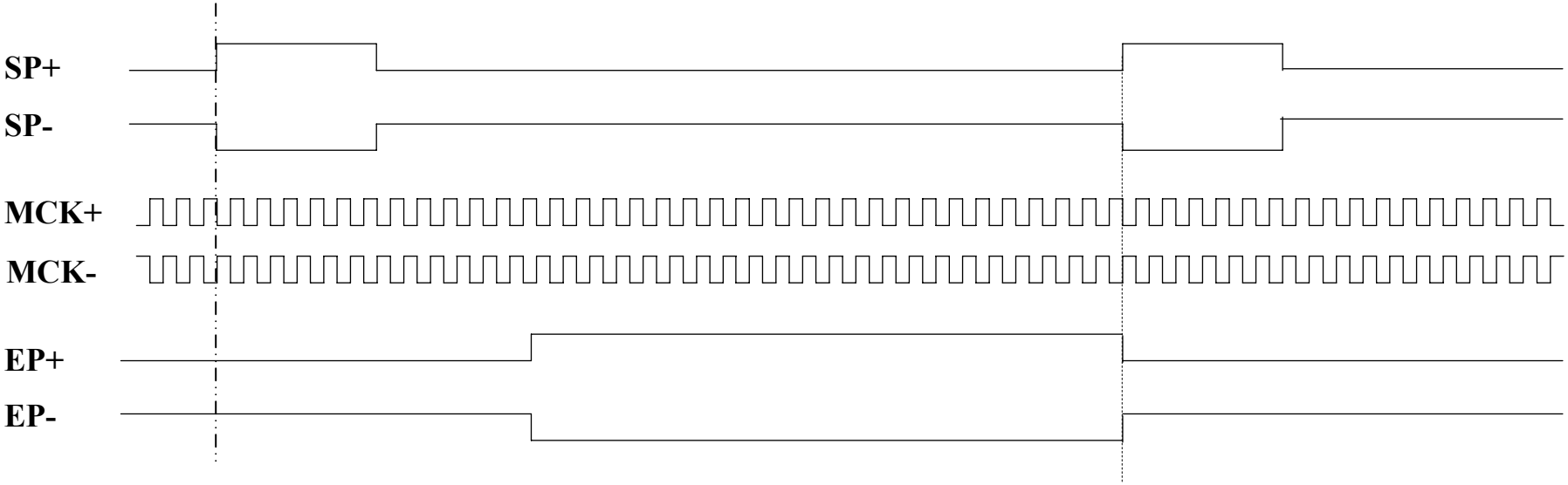


Figure 13. External interface of the C640 device

Timing Diagram for input clock

For Fr = 312.5 frames/s, input frequency = 12 x 1.293MHz, 1tp = 12ck, 1ck=64.45ns
(External Signals for Single Frame Capture and Multi-Frame Accumulate Mode)

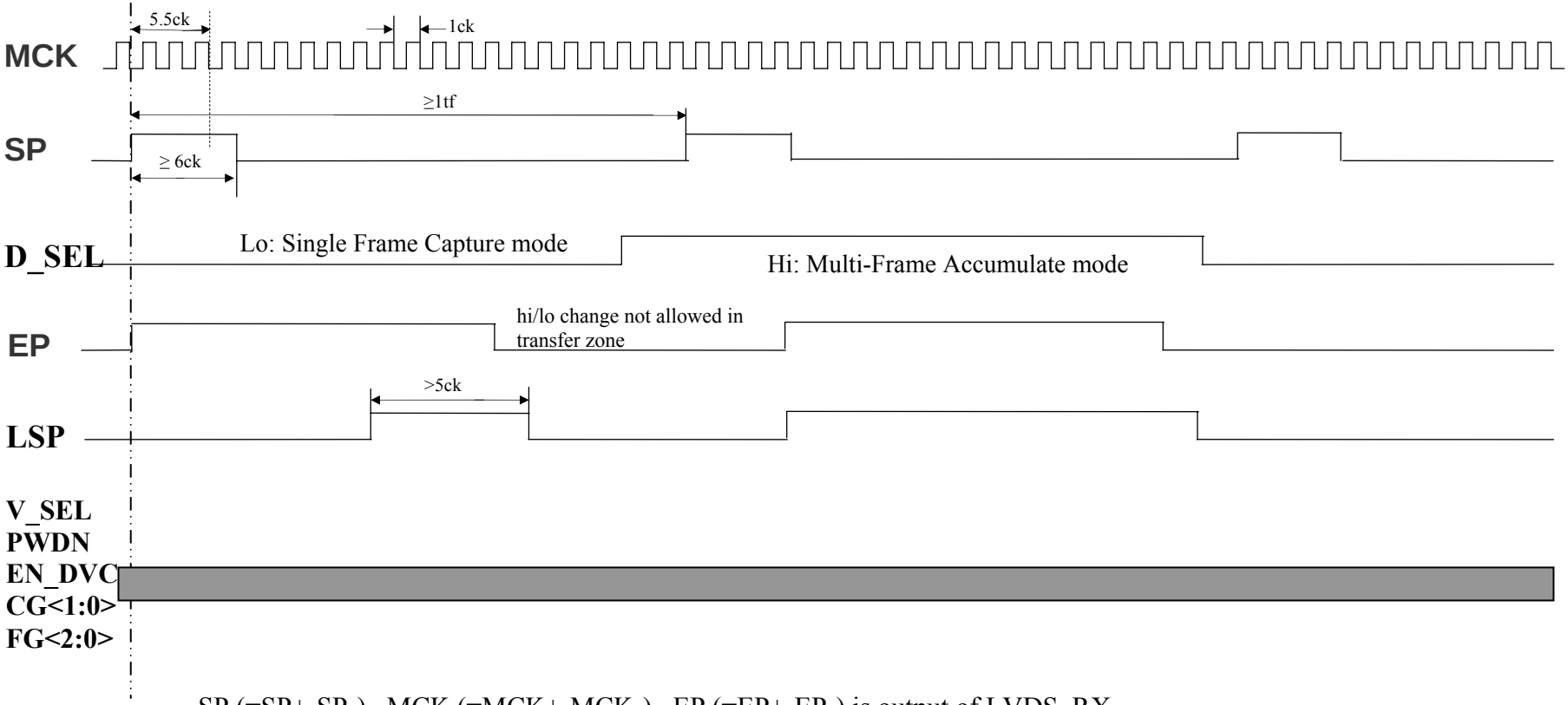
- **Differential Input Clocks (to LVDS_RX)**



- Edge coincidence for external SP and MCK is not necessary.
- EP is independent of MCK and SP in destructive mode.
- EP has relation with SP in non-destructive mode
- SP high duration need to cover at least 6 MCK clock cycle for the valid signal

Figure 14. Differential input clock pulse

Timing Diagram between input clock and latch input control



- SP (=SP+-SP-), MCK (=MCK+-MCK-), EP (=EP+-EP-) is output of LVDS_RX
- D_SEL, LSP, V_SEL, EN_DVC, CG<1:0>, FG<2:0> and PWDN are 3.3V CMOS inputs and independent of SP, MCK

Figure 15. Relationship between input clock pulse and latch input control

Output Timing Diagram

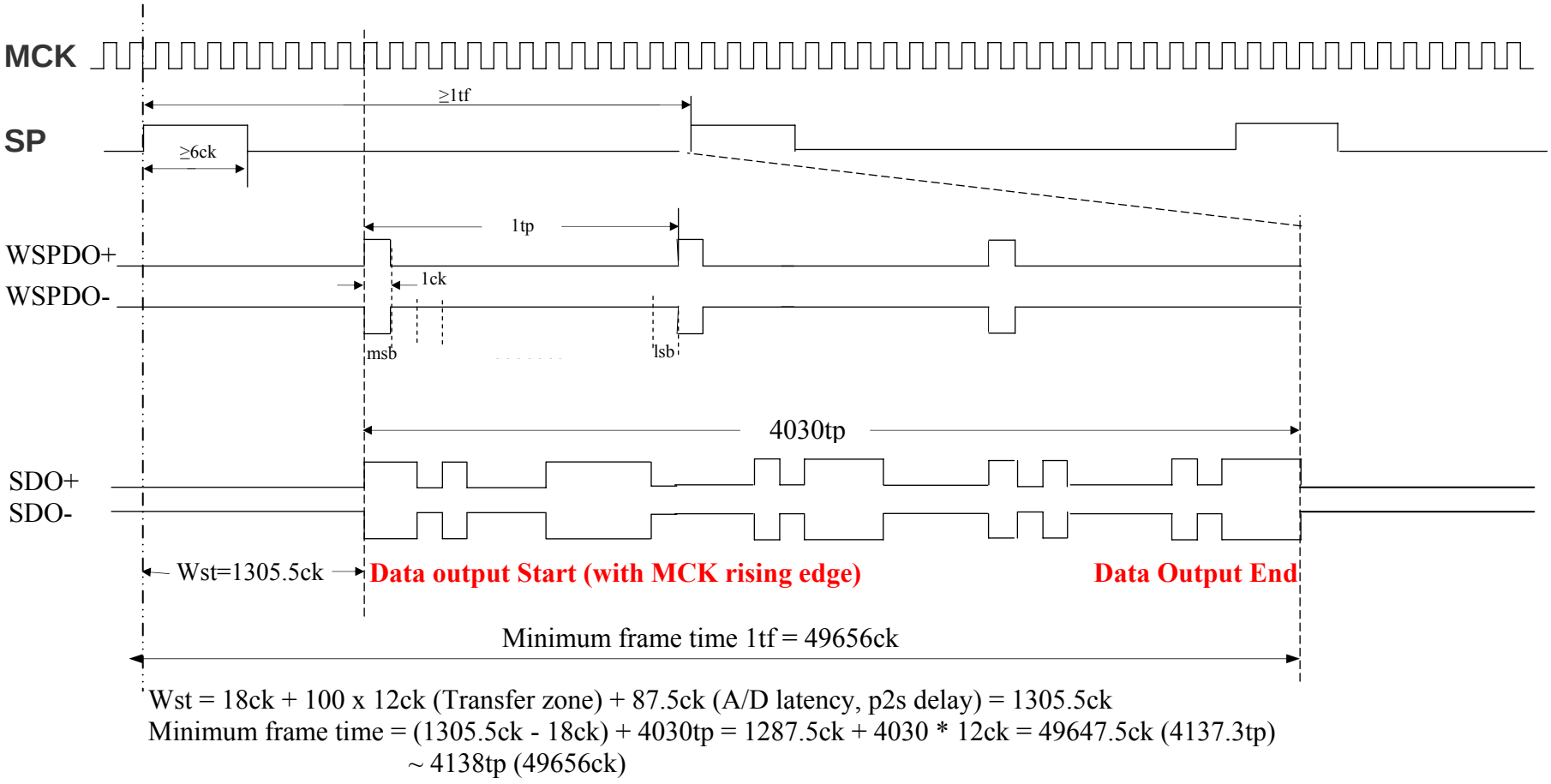


Figure 16. Output timing diagram

Data Output Timing relationship between EP and clock

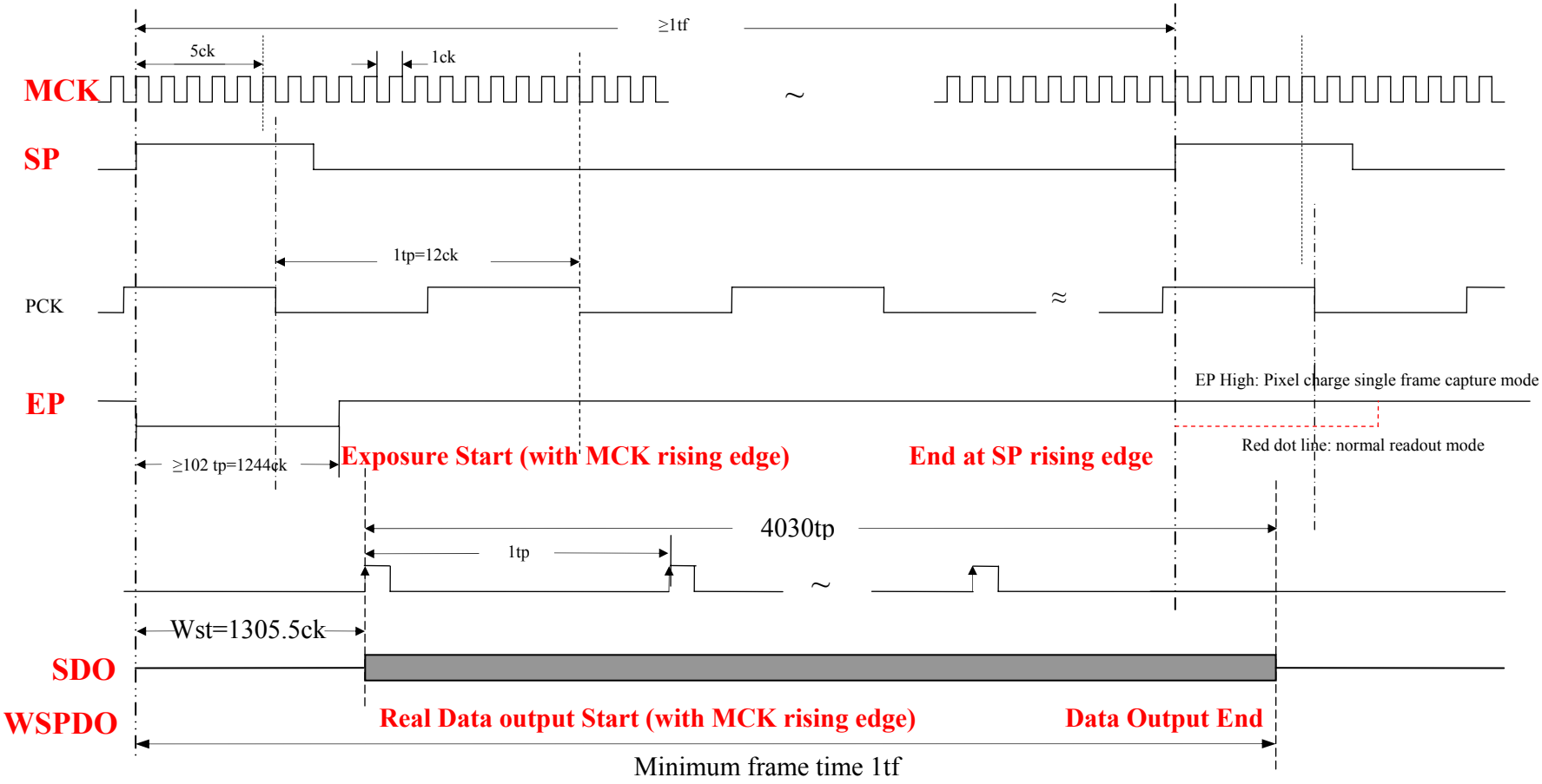
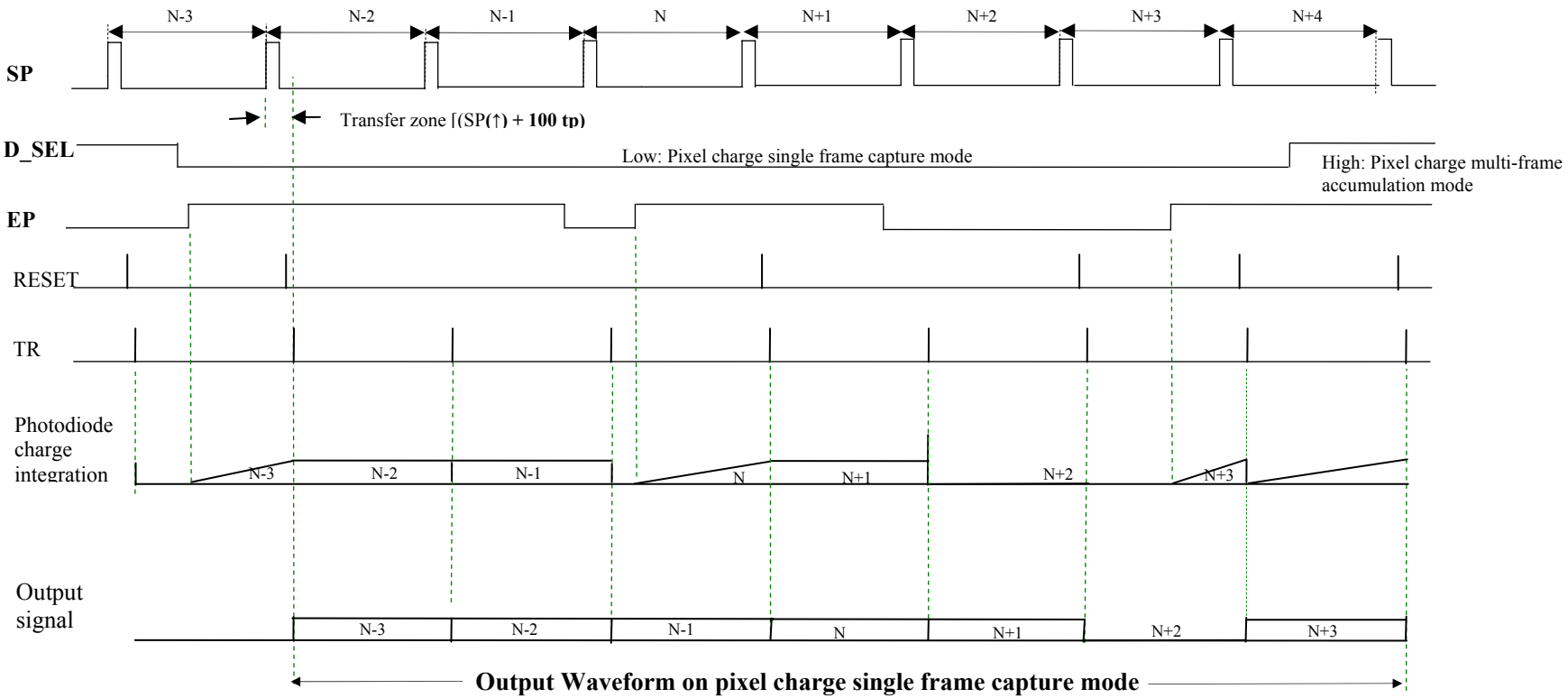


Figure 17. Timing diagram between EP, master clock, SP, and output data.

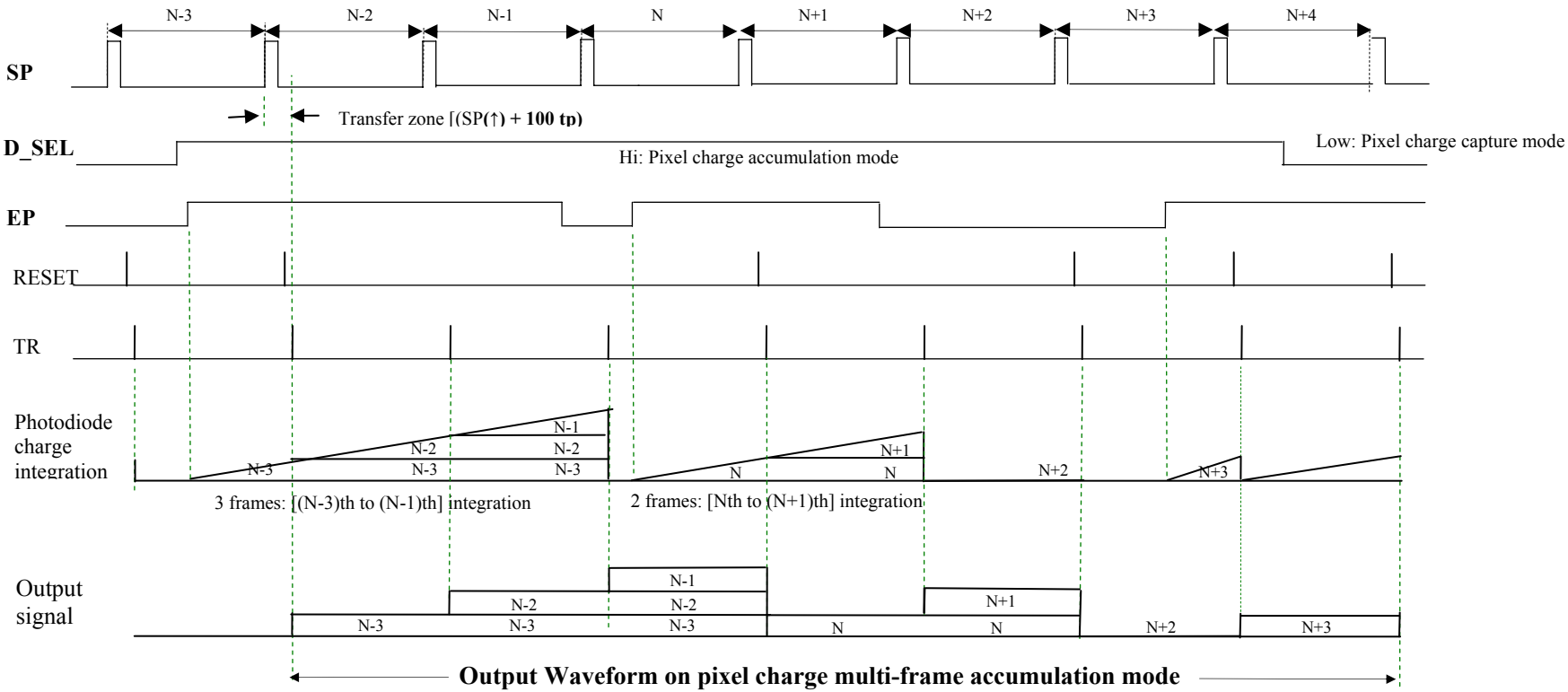
C640 timing diagram for pixel charge single-frame capture mode



1. **D_SEL should always be low during pixel charge single frame capture mode;**
2. **EP should not make transition in transfer zone;**
3. **EP Should go from low to high before SP(↑) and after previous transfer zone to initiate exposure in pixel charge single frame capture mode;**
4. **EP low, the photodiode does not accumulate any incident light or Dark current charge. Photodiode accumulates charge only when EP is high.**
5. **D_SEL and EP are independent of MCK.**

Figure 18. Timing diagram of the pixel charge single frame capture mode

C640 timing diagram for Multi-Frame pixel charge accumulation



1. **D_SEL should always be high during pixel charge multi-frame accumulation mode;**
2. **EP should not make transition in transfer zone;**
3. **EP Should go from low to high before SP(↑) and after previous transfer zone to initiate exposure in pixel charge multi-frame accumulation mode;**
4. **EP low, the photodiode does not accumulate any incident light or Dark current charge.**
5. **Photodiode accumulates charge only when EP is high, except when EP (High -> Low) before next SP(↑).**
6. **D_SEL and EP are independent of MCK.**

Figure 19. Timing diagram of the pixel charge multi-frame accumulation mode

Electrical characteristics of input / output pins

DC operating conditions (T = -15°C to 125°C)

Parameter	Symbol	Value			Units
		Min	Typ	Max	
Supply Voltage	VDD (Pin DVDD, VDD)	3.135	3.3	3.465	V
Active Supply Current	I_{VDD} I_{DVDD}			60 20	mA
Logic Hi	V_{IH}	0.7VDD		VDD+0.3	V
Logic Lo	V_{IL}	-0.3		0.3*VDD	V
Backup Reference Voltage	V_{REFP}		2.674		V

Table 4 DC operating conditions

CMOS Input / Output DC Electrical Characteristics

Input Pins: PWDN, CG<1:0>, FG<2:0>, V_SEL, D_SEL, EN_DVC
(3.135 V < VDD < 3.465V, T = -15 ˚C to +125 ˚C)

	Symbol	Condition	Value			Units
			Min	Typ	Max	
High Level Input Voltage	V_{IH}		0.7*VDD		VDD+0.3	V
Low Level Input Voltage	V_{IL}		-0.3		0.3*VDD	V
High Level Input Current	I_{IH}	Input Buffer, Vin=VDD	-10		10	uA
Low Level Input Current	I_{IL}	Input Buffer, Vin=VSS	-10		10	uA
Switching Threshold	V_{OH}	At 3.3 V power supply		1.5		V
High Level Output Voltage	V_{OH}	At 1.6 mA load	0.7*VDD			V
Low Level Output Voltage	V_{OL}	At 1.6 mA load			0.5	V

Table 5 CMOS input / output electrical characteristics

LVDS TX and RX DC Electrical Characteristics

LVDS_TX

Output Pins: WSPDO±, SDO± (3.135 V < VDD < 3.465V, T = -15 ˚C to +125 ˚C)

Parameter	Symbol	Conditions	Value			Units
			MIN	TYP	MAX	
Differential Voltage Swing	V_{OD}	RL=100 Ω	±300	±350	±400	mV
Change in Magnitude of V_{OD} for Complementary Output States	ΔV_{OD}				35	|mV|
Offset Voltage	V_{OS}		1.125	1.25	1.375	V
Change in Magnitude of V_{OS} for Complementary Output States	ΔV_{OS}				35	|mV|
Output High Voltage	V_{OH}				1.6	V
Output Low Voltage	I_{OL}		0.9			V
Output Driver Current	I_O		3.0	3.5	4.0	mA
Output Pins at Power Off	Z_O		High Impedance			

Table 6 LVDS DC electrical characteristics.

LVDS_RX

Input Pins: CLK±, EP±, SP± (3.135 V < VDD < 3.465 V, T = -15 ˚C to +125 ˚C)

Parameter	Symbol	Conditions	Value			Units
			MIN	TYP	MAX	
Differential Input High Threshold Voltage	V_{IH}	V_{CM}=1.25	-100			mV
Differential Input Low Threshold Voltage	V_{IL}				+100	mV
Common Mode Voltage Range	V_{CM}		0.6		2.3	V
Input Leakage Current	I_{LK}				20	uA

Table 7 LVDS RX electrical characteristics

6. DEVICE SPECIFICATION

6.1 Prime physical parameter specifications

6.1.1 Sensor chip

Item	Specification
Number of elements	4000 active 20 dummy at starting and 10 dummy at end for automatic dark signal correction
Element Pitch	7 μm
Element size	7 μm x 7 μm (active area size)
No. of video ports	Single

6.1.2 Package

Item	Specification
Package style	Ceramic Dual in line package (DIP), Hermetically sealed
Mounting Mechanism	The detector has two mounting holes. One hole on each side of the package.

6.1.3 Glass window

Item	Specification
Material	D263T
Thickness	1.1 ± 0.1mm
Flatness	10 um maximum
Parallelism	20 um maximum
AR coating	Double side coating. Reflectance less than 4% in the spectral zone 450nm to 900nm.
Surface quality	Scratch: 100 um maximum; Dip: 10 um maximum

6.1.4 Sealing:

Hermetic seal.

6.2 Electrical and electro-optical parameter specifications

Item	Specification
Readout mode	Read while integrate Start and stop integration of all pixels should be simultaneous (snap shot)
Integration time (Ti)	1 ms ~ 32 ms per frame
Frame rate (Fr)	32 ~ 1000 frames per second
Pixel clock frequency	4 MHz ~ 125 k Hz

Master clock frequency	48 MHz ~ 1.5 MHz
Dark Current	⩽ 50 DN/sec/pixel for all pixels of the array
Noise floor in dark	⩽ 1.5 DN (300 e)
Conversion rate	200 e / DN
Full well capacity	⩾ 720 ke
SNR @ Gain = 1	⩾ 2000
PSRR of the device	⩾ 60dB on all the supply lines at 2xFr readout frequency
Power consumption	⩽ 250 mW at 2x Fr readout frequency
Spectral response	6000 DN/(uJ/cm^2) in the spectral response band of 450nm to 900nm
Dark offset mean	⩽ 3 DN at integration time Ti = 3.2 ms
Dark offset non-uniformity	⩽ 1 DN RMS including FPN
Residue (Line to Line)	⩽ 1% when alternate Lines are illuminated up to 90% of Full Well
Non-linearity at digital output	⩽ 1% in 10% to 90% of Full Well for any pixel ⩽ 2% outside this range
Maximum non-uniformity	⩽ 1% RMS including fixed pattern noise (FPN)
Anti-blooming	> 10 times of saturation with build in anti-blooming circuitry.

7. ABSOLUTE MAXIMUM RATINGS

Analog power supply voltage, VDD ---------- 4.0 V
Analog power supply current, I_{VDD} ---------- 80 mA
Digital power supply voltage, DVDD ---------- 4.0 V
Digital power supply current I_{DVDD} ---------- 30 mA
LVDS RX input voltage range ---------- 0.6 to 1.9 V
CMOS Digital input voltage range, Vih ---------- -0.3 to VDD +0.3 V
Operating free-air temperature range, Ta ---------- -15 °C ~ 85 °C
Storage temperature range, Tstg ---------- -15 °C ~ 125 °C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8. RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Unit
Analog Power supply voltage	VDD	3.135	3.3	3.465	V
Analog Power supply current	I_{VDD}		65		mA
Digital power supply voltage	DVDD	3.135	3.3	3.465	V
Digital power supply current	I_{DVDD}		15		mA
LVDS RX common mode voltage	V_{CM}	0.9	1.25	1.6	V
LVDS RX differential voltage	Vdffin	V_{CM} –0.3	0.35	V_{CM} +0.4	V
CMOS High level input voltage	V_{ih}	VDD x 0.7		VDD+0.3	V
CMOS Low level input voltage	V_{iL}	0		VDD x 0.3	V
Clock frequency	f	0.1	2	5	MHz

Sensor integration time	t_{int}	1.6	3.2	512	ms
Wavelength of light source	λ	400		900	nm
Clock pulse high duty cycle		30		70	%
Operating free-air temperature	T_A	-15		125	°C

9. PIN DESCRIPTION AND PACKAGE

The following shows the pin description for C640.

Pin No	Pin Name	Type	Function description
1	AVDD	P	Analog power supply; 3.3 V
2	CLK+	LVDS-I	Master clock input pulse, LVDS (+)
3	CLK-	LVDS-I	Master clock input pulse, LVDS (-)
4	SP+	LVDS-I	Start pulse input, LVDS (+)
5	SP-	LVDS-I	Start pulse input, LVDS (-)
6	EP+	LVDS-I	Exposure control pulse input, LVDS (+)
7	EP-	LVDS-I	Exposure control pulse input, LVDS (-)
8	SDO-	LVDS-O	Video signal data output, LVDS (-)
9	SDO +	LVDS-O	Video signal data output, LVDS (+)
10	WSPDO+	LVDS-O	Word start output, LVDS (+)
11	WSPDO -	LVDS-O	Word start output, LVDS (-)
12	AVDD	P	Analog power supply voltage; 3.3 V
13	REFP	AO	Reference voltage output
14	VI	AI	External input voltage; For testing ADC performance only
15	AVSS	P	Analog ground; 0 V
16	AVDD	P	Analog power supply voltage; 3.3 V
17	DVSS	P	Digital ground
18	DVDD	P	Digital power supply
19	PWDN	DI	Power down
20	LSP	DI	Latch start pulse input
21	D_SEL	DI	Single Frame / Multi-Frame mode selection; Lo: Single Frame Capture, Hi: Multi-Frame Accumulate
22	CG<1>	DI	Coarse gain control, bit 1
23	CG<0>	DI	Coarse gain control, bit 0

24	FG<2>	DI	Fine gain control, bit 2
25	FG<1>	DI	Fine gain control , bit 1
26	FG<0>	DI	Fine gain control, bit 0
27	EN_DVC	DI	Dark voltage cancellation (DVC) selection; Lo: disable, Hi: enable
28	V_SEL	DI	External input voltage selection. Lo: disable, Hi: enable
29	AVSS	P	Analog ground; 0 V
30	AVSS	P	Analog ground; 0 V

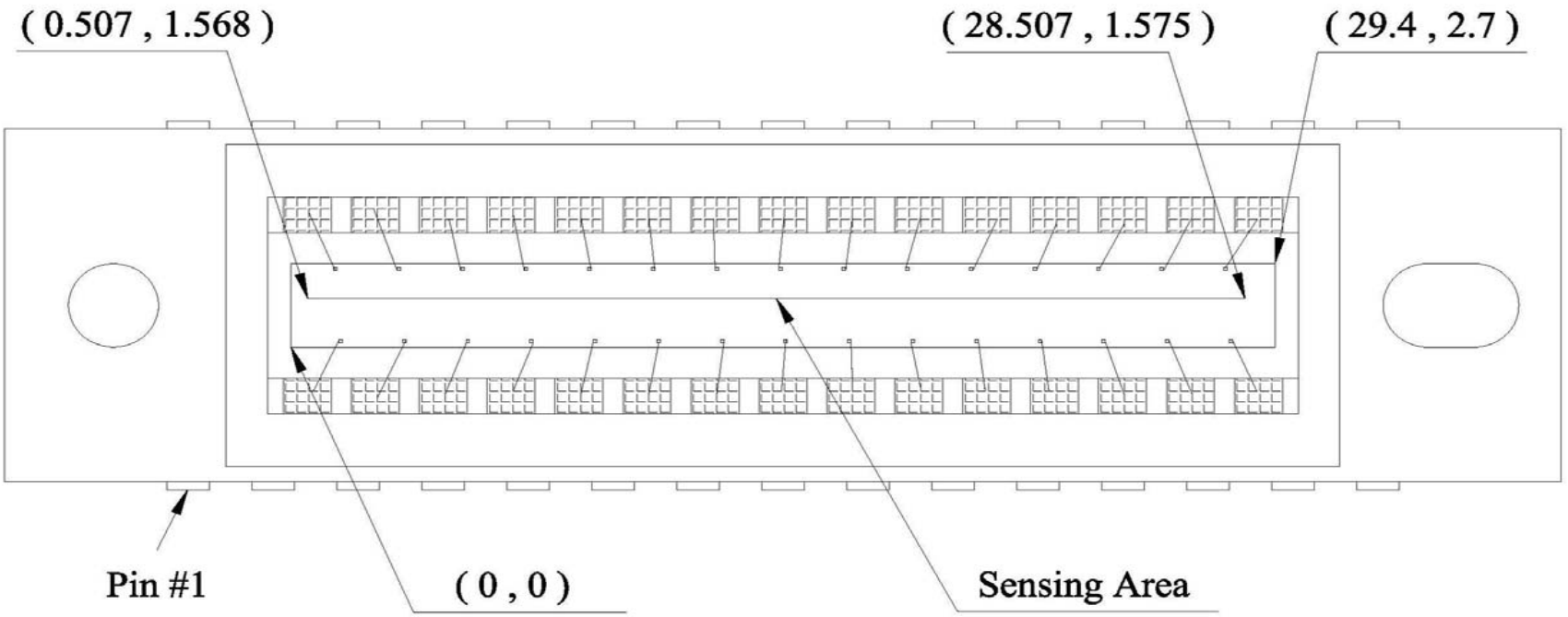


Figure 20. Chip location on the ceramic package (unit is mm).

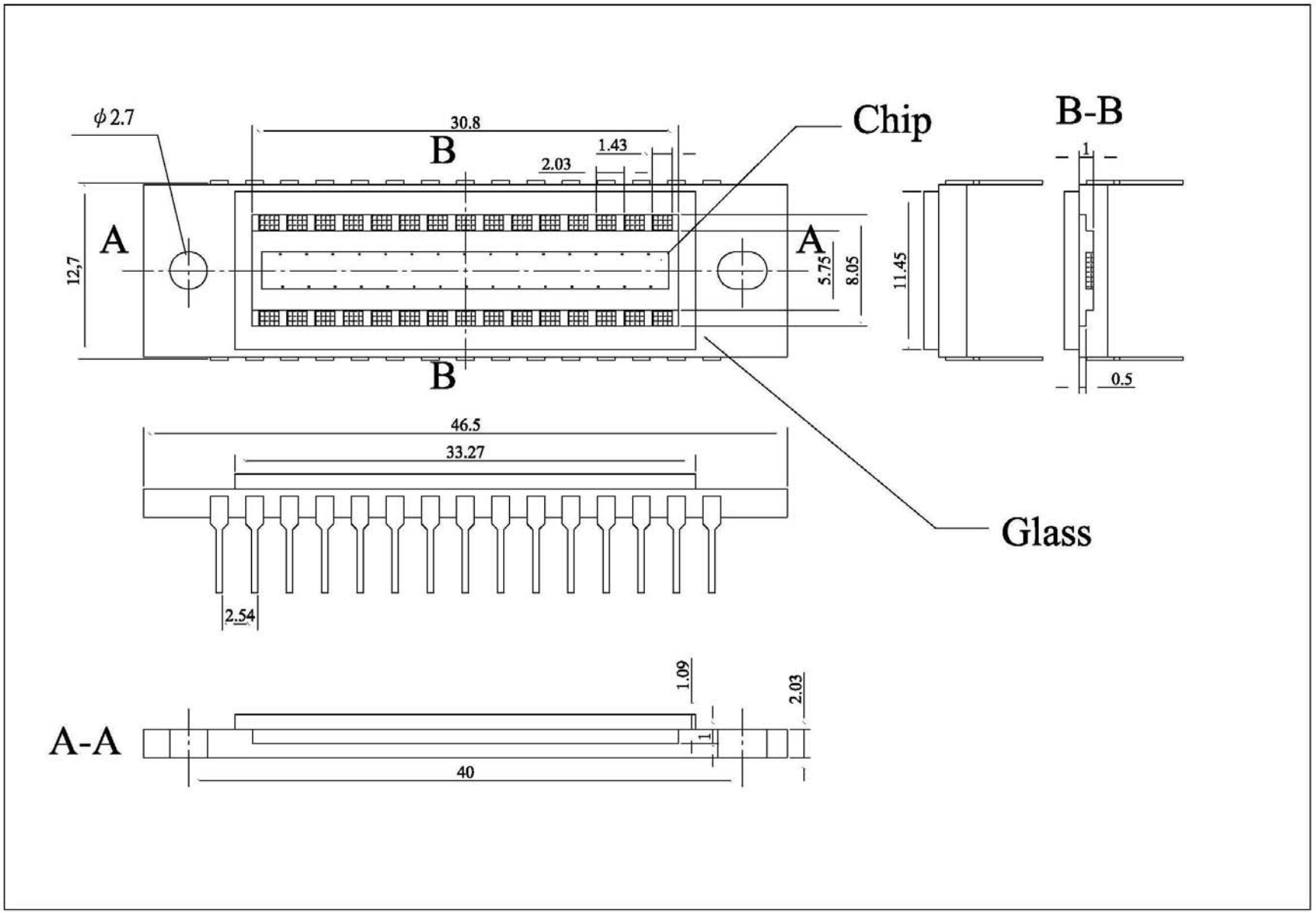


Figure 21. Package drawing of the C640 device.

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