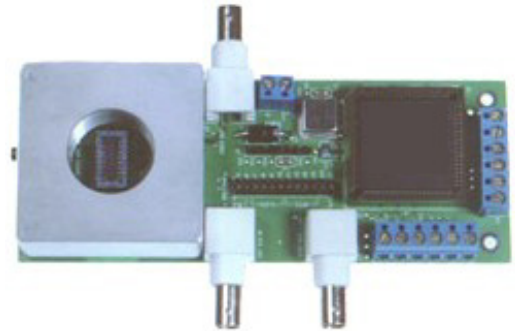


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LIS DEMO KIT FOR LIS-1024 Image Sensor

Demonstrates capabilities of LIS 1024 image sensor. Refer to the latest LIS-1024 product specification available from our web site for details on these imagers.

- Pixel read rate selectable in 16 increments from 610 to 20 MHz
- Integration time selectable in 16 increments from 1 frame to 32768 frames of video, non destructive read mode.
- Demonstrates Imagers capability for Dynamic Pixel Reset™, destructive read and non-destructive read modes.
- Demonstrates device timing as an aid to developers.



Description

The LIS demonstration kit is designed to display the capabilities of the LIS-1024 image sensor. A CPLD is used to interpret user device settings and generate the necessary timing to the imager. The CPLD automatically configures itself to the imager model installed. The imager is socketed, so the user can interchange imagers at will.

The user can select the reset mode, read clock frequency, and integration time via simple plug on jumpers. For a minimum configuration, the user need only supply 5.0 VDC, dual trace oscilloscope with external trigger capability or data acquisition device to display or capture the analog video, a load for the video out, and a light source. Analog video out from the LIS series of imagers is from 0.74 (typical) at dark to 3.8 VDC Saturated typical.

Provision is provided for the user to mount a load resistor, or the user can connect the video out to an external load. A load should be connected for the device to operate properly. Care should be taken to provide the correct load to the imager. See the latest revision of LIS-1024 specification document PDS0001 REV X for details. This document can be downloaded from our web site at www.panavisionsvi.com. In addition, the user may wish to put a band width filter on the output video. The use of a lens is suggested, and an optional CS lens mount adapter is available as an option.

BNC and screw terminal connectors are provided so that the user may monitor device timing, or optionally, provide their own timing signals.

Should additional capabilities be desired, the kit is provided with a programming port so that the CPLD can be re-programmed to suit the users needs. SVI does not provide user programming support, but does offer a programming service. User programming support can be obtained from the CPLD manufacturer and/or suppliers of CPLD programming software.

Product LIS Demo Kit

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Electrical Characteristics/Operating Conditions

Parameter	Notes	Min	Typical	Max	Units
Supply Voltage		4.85	5.0	5.25	V
Power Consumption			500	650	mW
Input High Level			2.5		V
Input Low Level			0.7		V
Pixel Read Rate	User selectable in 6 increments (see jumper settings) and depends on BASE crystal frequency installed.	0.610		20,000	khz

Absolute maximum ratings, T A = 25°C unless otherwise noted, see Note †

Supply voltage range, -----V_{DD} 0 V to 5.25 V
 Digital input current range, I ----- -20 mA to 20 mA
 Operating case temperature range, T_C (see Note 2)----- -10°C to 70°
 Operating free-air temperature range, T_A ----- 0°C to 50°C
 Storage temperature range ----- -20°C to 85°C
 Humidity range, Rh ----- 0-100%, non-condensing

† Exceeding the ranges specified under “absolute maximum ratings” can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated under “recommended operating conditions” is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.

NOTES: 1. Voltage values are with respect to the device GND terminal.

2. Case temperature is defined as the surface temperature of the package measured directly over the integrated circuit.

PART NUMBER DETERMINATION

Part Number: LIS: DBD-001-B

LIS-1024 Demo kit with LIS-1024 imager installed.

OPERATING INSTRUCTIONS

These instructions describe use with a dual trace oscilloscope with external trigger capability. A nice feature to also have on the scope is a delay. It is assumed that the user is familiar with the operation of their oscilloscope.

1. Set the jumpers, J5-J12, J18, and J19 for the desired operating parameters. See Jumper settings, below.
2. Connect appropriate load resistor between E13 and E14 or connect J3 to an external load. See the latest LIS-1024 product specification document PDS0001 for load range. Provisions are also provided to add a series load or filtering. This can be done by cutting the trace between E11 and E12 on the component side of the kit, and installing your desired component(s).
3. With power off, connect 5 VDC to J13-1 and Ground to J13-2. Ensure polarity is correct, or damage to the kit and/or user power supply is possible.
4. Connect the Master Clock (Pixel read rate) (J4) to scope channel 1, if observation of clock is desired.
5. Connect the Video out (J3) to scope channel 2.
6. If you are using the destructive read mode, or only wish to view one frame of video at a time, connect the SYNC out (J17) to the external trigger input of your scope. SYNC out occurs at the end of every frame. If you are using the kit for multiple frames of integration, connect the external trigger of your scope to screw terminal J1-3, Pixel Reset. Pixel reset is pulsed at the end of the integration time as setup by jumpers J11, J12, J18, and J19.
7. Set the vertical scale of the scope to display a 0-5 VDC signal, typically 1 V/Div.
8. Set the horizontal (time base) to display the number of frames chosen for the integration time.
9. All should be set for operation. Power up your scope and power supply. You can monitor device timing issues, zoom in the video, and display individual pixel data if desired. It is of course not necessary to display both channels simultaneously. Please note that the best time to perform an A/D function for your product or data acquisition system would be during the second half of the pixel time.

The next page illustrates various oscilloscope traces that were captured using the demo kit. The traces indicate the horizontal and vertical settings.

Note that some traces show a spike between frames of video. This is of no concern and is caused by the video bus floating between frames. Note that the spikes are present but not displayed for non-destructive read mode traces. The reason they are not displayed is that the digital scope used to capture these images has a slow sample rate.

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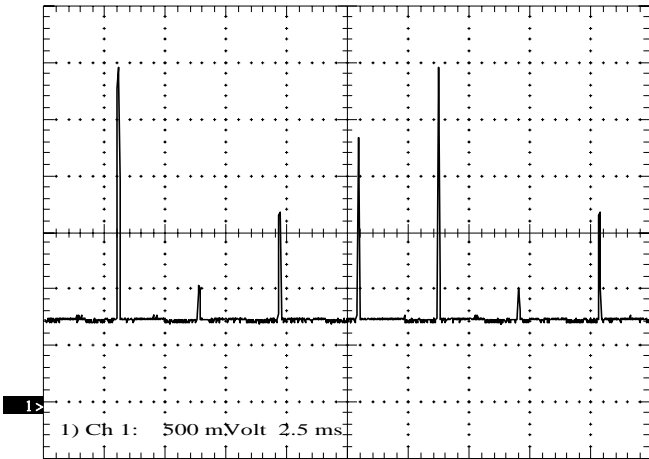


Figure 1: Non-destructive read, point light source 156.25KHz, 4 Frames Integration

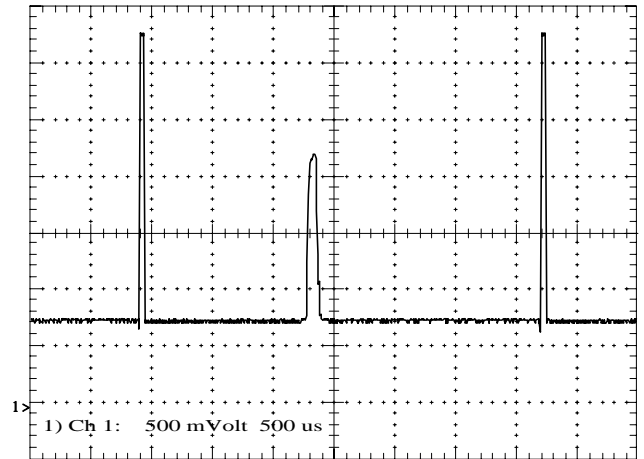


Figure 2: Destructive read, point light source 156.2KHz, DPR mode, 1 frame. Note end of frame spikes caused by floating video bus.

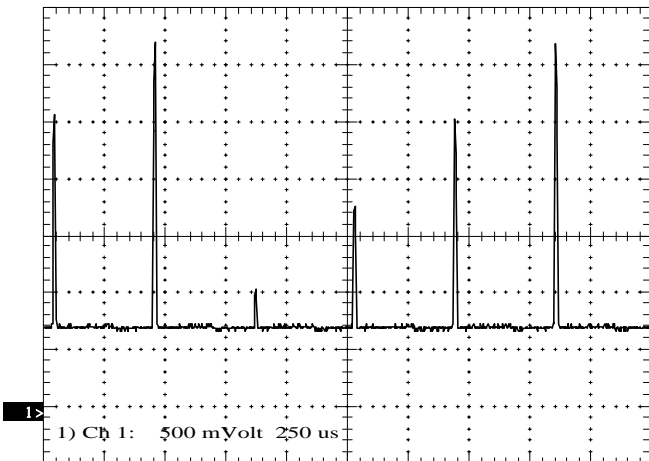


Figure 3: Non-destructive read, point light source light source 1.25 MHz 4 Frames Integration

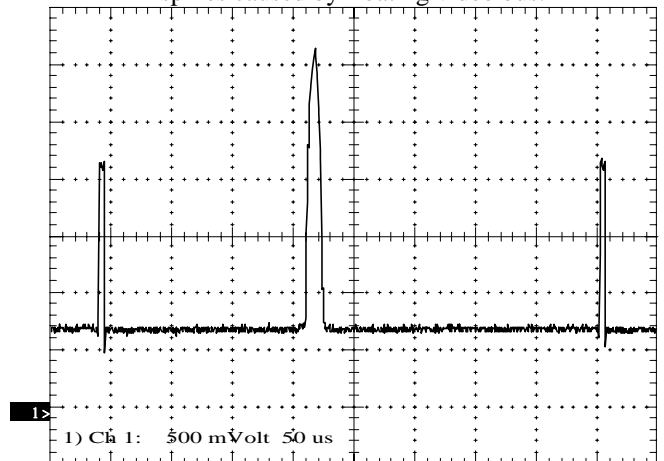


Figure 4: Destructive read, point 1.25 MHz DPR mode, 1 frame.

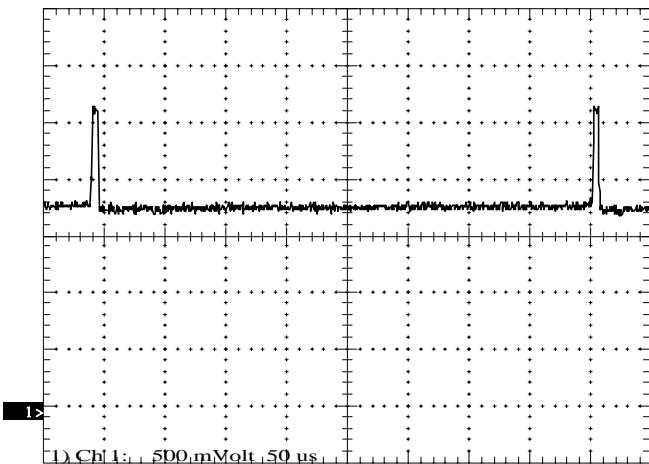


Figure 5: Destructive read, single frame 1.25 MHz DPR mode 40% light level.

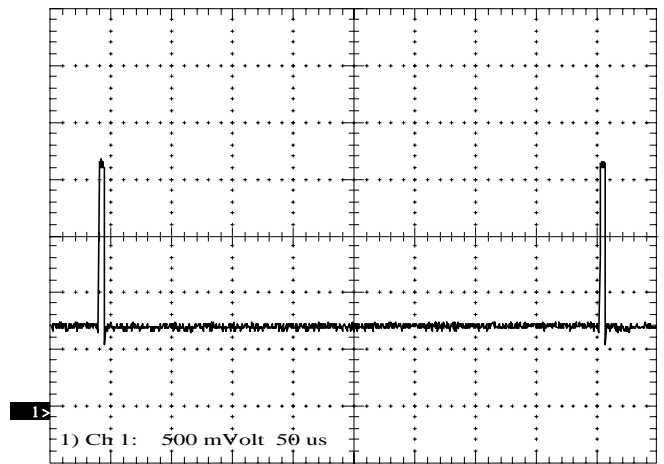


Figure 6: Destructive read, single frame 1.25 MHz DPR mode 0% light level.

JUMPER SETTINGS

Jumpers J5 through J21 are user selectable settings. These are as follows;

J5	Sets up Reset Mode as Dynamic Pixel Reset™ (Sequential) or Frame.
J6	Sets up destructive or non-destructive read out.
J7-J10	Sets up the clock speed to the imager.
J11-J12, J18-J19	Sets up integration time for imager, as number of frames to integrate.
J20	Unused
J21	Reserved

Note:

ON – means jumper is in place.

OFF – means jumper is removed.

Jumpers J5 and J6

Reset Mode and Read select

Jumper	OFF setting	ON setting	Default setting
J5	DPR™ mode	Frame mode	ON
J6	Destructive read	Non-Destructive read	ON

Note: Valid settings are either both J5 and J6 jumpers ON or both OFF.
Combination settings not valid.

Jumpers J7-J9

Clock Speed or pixel read rate

J7	J8	J9	J10	Clock speed	Pixel Clock	Comment
ON	ON	ON	ON	BASE÷2	20 MHz*	Default
OFF	ON	ON	ON	BASE÷4	10 MHz	
ON	OFF	ON	ON	BASE÷8	5 MHz	
OFF	OFF	ON	ON	BASE÷16	2.5 MHz	
ON	ON	OFF	ON	BASE÷32	1.25 MHz	
OFF	ON	OFF	ON	BASE÷64	625 kHz	
ON	OFF	OFF	ON	BASE÷128	312.5 kHz	
OFF	OFF	OFF	ON	BASE÷256	156.25 kHz	
ON	ON	ON	OFF	BASE÷512	78.125 kHz	
OFF	ON	ON	OFF	BASE÷1024	39.063 kHz	
ON	OFF	ON	OFF	BASE÷2048	19.530 kHz	
OFF	OFF	ON	OFF	BASE÷4096	9.766 kHz	
ON	ON	OFF	OFF	BASE÷8192	4.883 kHz	
OFF	ON	OFF	OFF	BASE÷16384	2.441 kHz	
ON	OFF	OFF	OFF	BASE÷32768	1.221 kHz	
OFF	OFF	OFF	OFF	BASE÷65536	0.610 kHz	

Other jumper settings not shown are not supported. BASE frequency is 40 MHz.

*Imagers may not operate properly in DPR™ mode at this frequency.

Product LIS Demo Kit

Jumpers J11, J12, J18, J19

Frames of Integration

J11	J12	J18	J19	Frames of Integration	Comment
ON	ON	ON	ON	1	default
OFF	ON	ON	ON	2	Total Integration time is based on the following equation: $T_{int} = (1024+4) \times \text{Clock period} \times \text{frames of integration}$
ON	OFF	ON	ON	4	
OFF	OFF	ON	ON	8	
ON	ON	OFF	ON	16	
OFF	ON	OFF	ON	32	
ON	OFF	OFF	ON	64	
OFF	OFF	OFF	ON	128	
ON	ON	ON	OFF	256	
OFF	ON	ON	OFF	512	
ON	OFF	ON	OFF	1024	
OFF	OFF	ON	OFF	2048	
ON	ON	OFF	OFF	4096	
OFF	ON	OFF	OFF	8192	
ON	OFF	OFF	OFF	16384	
OFF	OFF	OFF	OFF	32768	

Example:

LIS-1024 with read rate set to 625khz with 128 frames of integration.

$$T_{int} = (1024+4) \times 1/625000 \times 128$$

$$T_{int} = 210 \text{ ms}$$

CONNECTORS

J1 – 6 position screw terminal - User interface for user I/O.

This connector provides access to the CPLD additional I/O. This I/O is not used for the base demo, but can be used with a user provided program.

TERMINAL	DESCRIPTION	COMMENT
J1-1	CPLD I/O 10	RMS - Reset Mode Select *
J1-2	CPLD I/O 11	RST - Reset *
J1-3	CPLD I/O 12	PRE - Pixel Reset Enable *
J1-4	CPLD I/O 13	Available user I/O
J1-5	CPLD I/O 14	Available user I/O
J1-6	GND	

*NOTE: Output signals only when CPLD is in MASTER mode. These terminals can be used to monitor the indicated signal. Board Revision 20005-1 pins J1-1 through J1-3 are incorrectly labeled. Use pin descriptions as above. New board, 20005-A is correctly labeled, as above.

J2 – 8 Single in-line header - In circuit programming port for CPLD. Refer to the CPLD manufacturer data sheets for the device and programming.

PIN	DESCRIPTION	COMMENT
J2-1	5 VDC	5 VDC PROGRAM PORT POWER
J2-2	SDOUT	SERIAL DATA OUT
J2-3	SDIN	SERIAL DATA IN
J2-4	/ISPEN	PROGRAM ENABLE (ACTIVE LOW)
J2-5	N/C	DO NOT CONNECT
J2-6	MODE	MODE SELECT
J2-7	GND	POWER SUPPLY GROUND
J2-8	SCLK	SERIAL CLOCK

J3 – BNC connector – Video out

J4 – BNC connector – Master Imager clock – 5 VDC TTL square wave generated by CPLD. Frequency set by user jumpers J7-J9. See Jumper Settings section for details.

J5-J12 – user jumper settings – See Jumper Settings section for details.

J13 – 2 position screw terminal. DC IN

TERMINAL	DESCRIPTION	COMMENTS
J13-1	5 VDC	DC 5VDC
J13-2	GND	POWER GROUND

Product LIS Demo Kit

J14 - 6 position screw terminal - Additional I/O - requires additional programming to use.

TERMINAL	DESCRIPTION	COMMENTS
J14-1	GND	
J14-2	CPLD I/O_2	USER I/O
J14-3	CPLD I/O_3	USER I/O
J14-4	CPLD I/O_4	USER I/O
J14-5	CPLD I/O_5	USER I/O
J14-6	GND	USER I/O

J17 – BNC connector – Sync out pulse. 5 VDC TTL output from imager, fired at end of frame. See LIS-1024 specification for details.

J18-J19 - Jumpers, works in conjunction with J11 and J12 to setup integration time. See chart above.

J20- not used

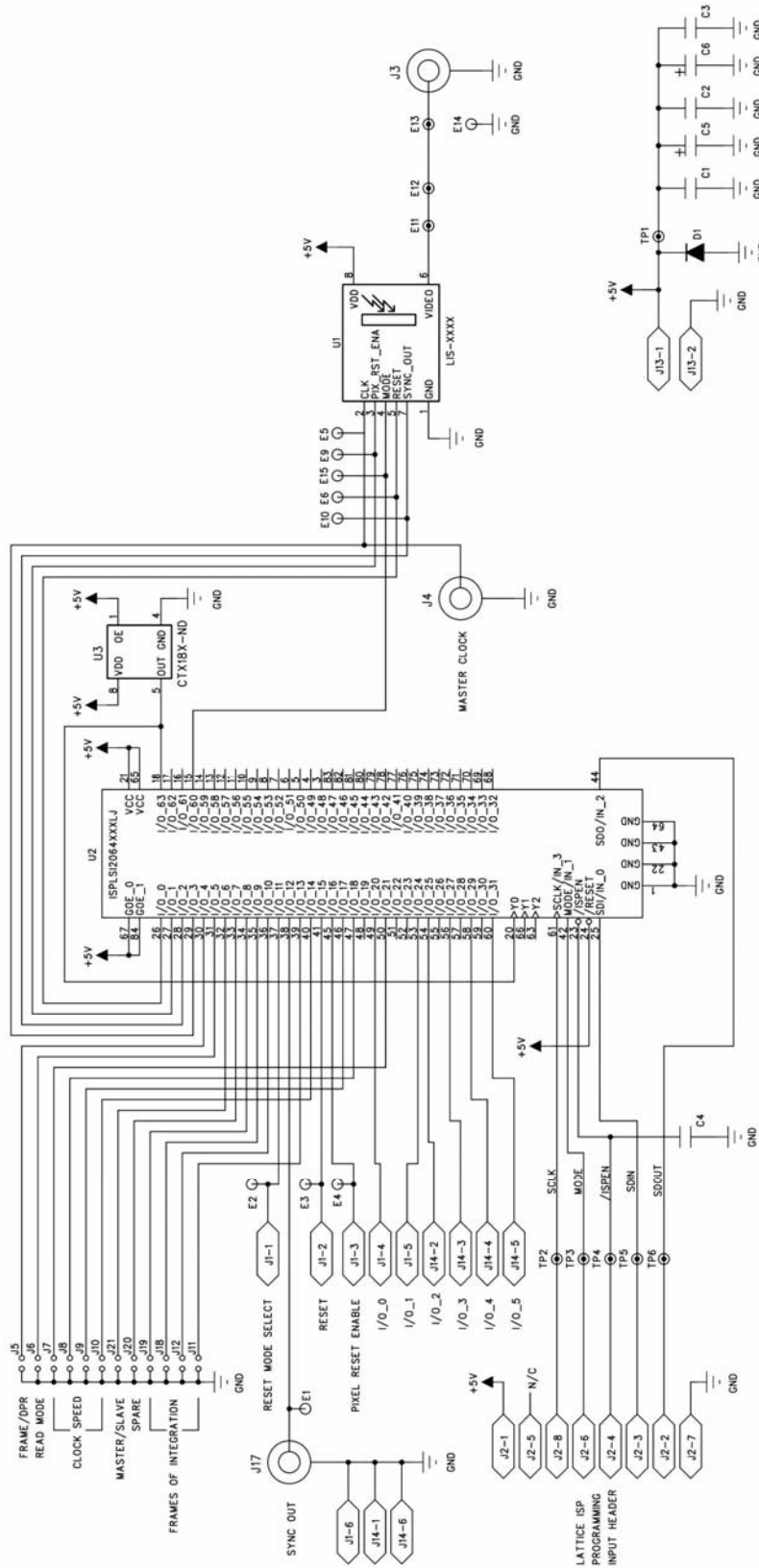
J21- Reserved

Installation of series load or band base filter.

Provision is provided to add a series load or band pass filter to the video out signal. This can be done by cutting the trace between E11 and E12, and then soldering in the series load or filter at E11 and E12

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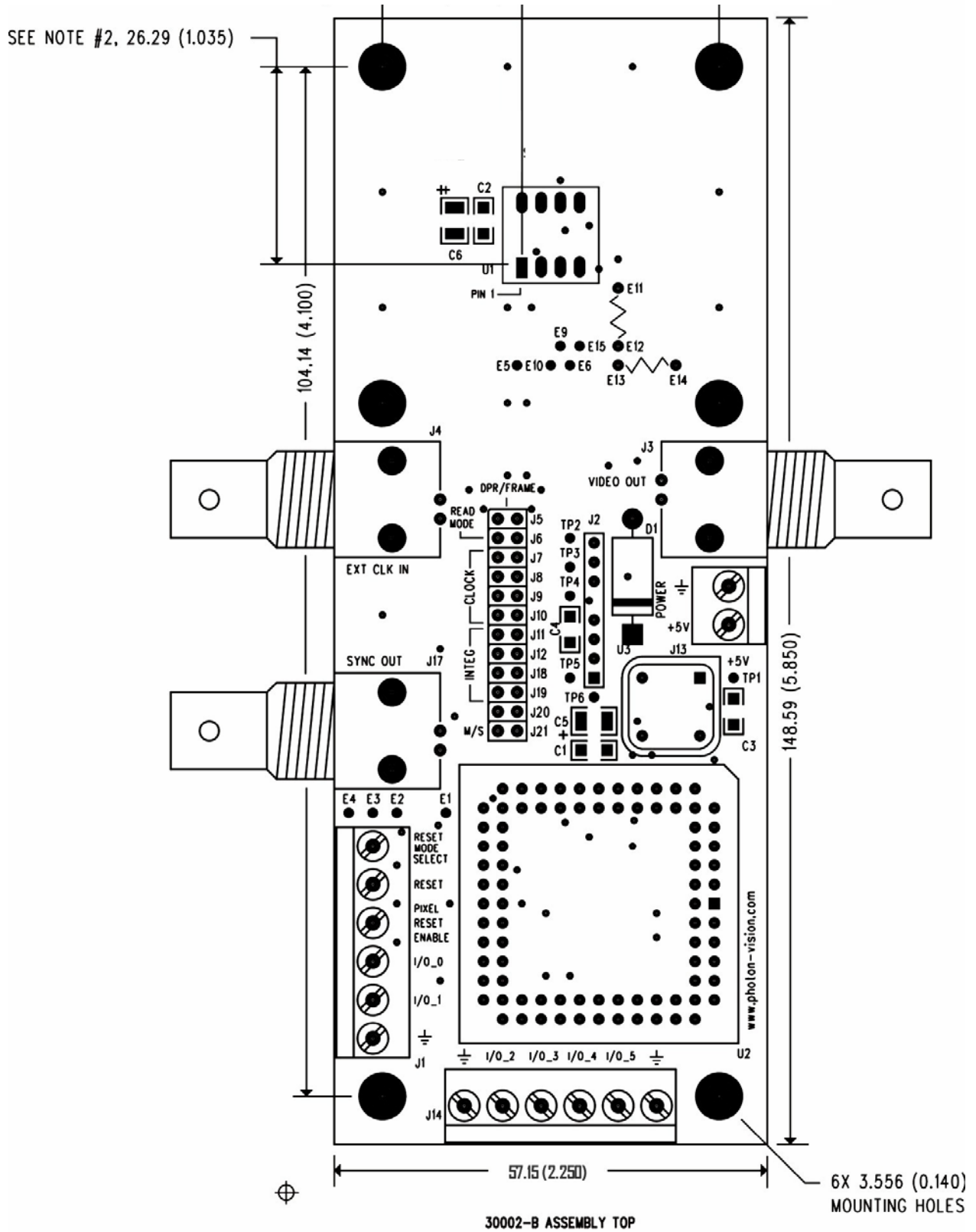
Electrical Schematic - For reference only.



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Product LIS Demo Kit

Layout drawing - For reference only.



Product LIS Demo Kit

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