

iC-LF

128x1 LINEAR IMAGE SENSOR

target specification



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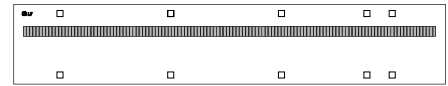
FEATURES

- ◆ 128 active pixels with $56\mu\text{m} \times 200\mu\text{m}$ photodiodes in a $63.5\mu\text{m}$ pitch (400DPI)
- ◆ Integrating L-V conversion followed by a sample-and-hold circuit
- ◆ High sensitivity and uniformity over wavelength
- ◆ High clock rates of up to 5MHz
- ◆ Shutter function enables flexible integration times
- ◆ Push-Pull output amplifier
- ◆ 5V single supply operation
- ◆ Can run off external bias to reduce power consumption
- ◆ Functions equivalent to and pin-to-pin compatible with TSL1401 (in an 8-pin oLGA LF2C package)

APPLICATIONS

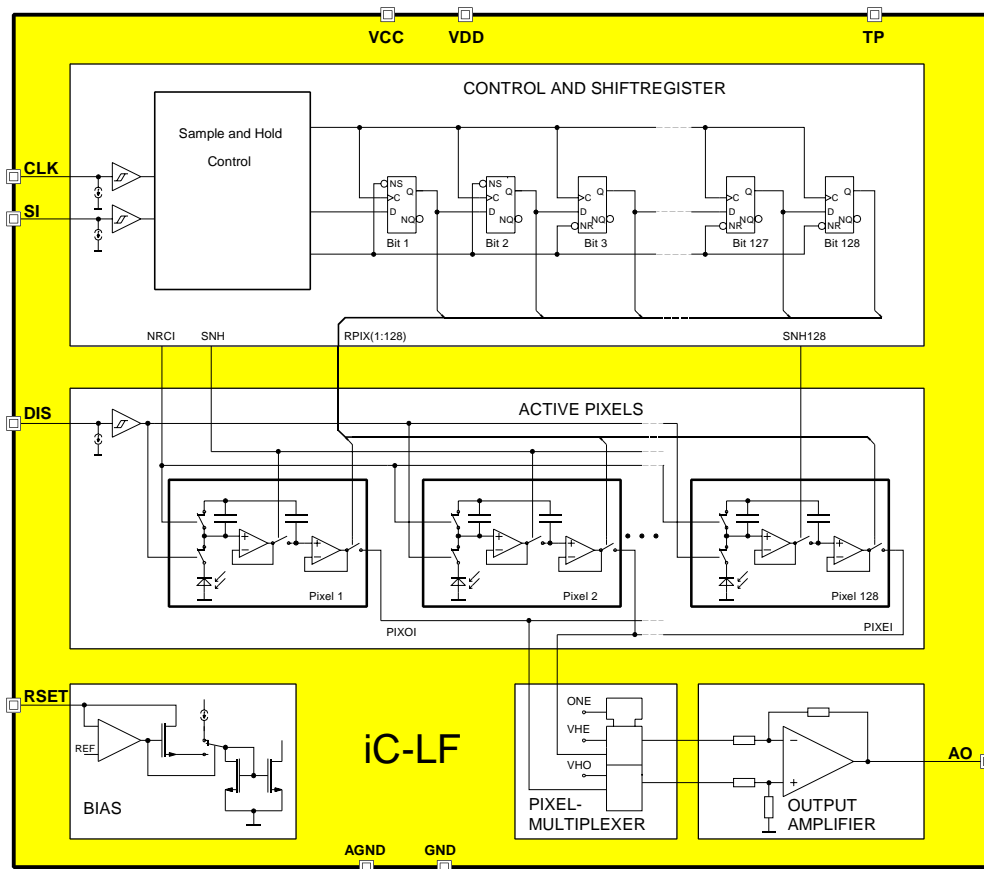
- ◆ Optical row sensors
- ◆ CCD substitute

PACKAGES



chip size 8.5mm x 1.6mm

BLOCK DIAGRAM



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DESCRIPTION

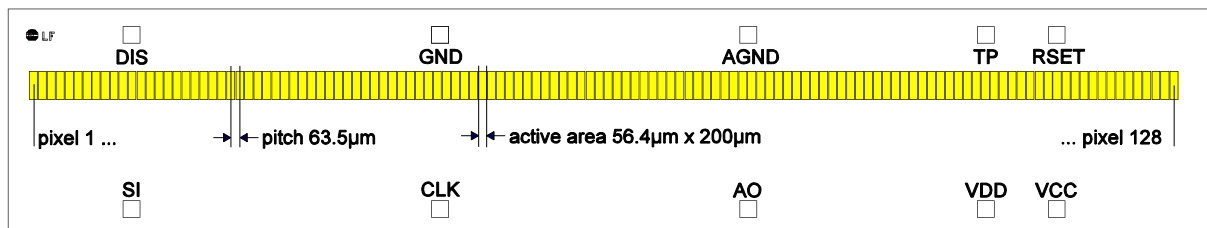
iC-LF is an integrating light-to-voltage converter with a row of 128 pixels pitched at $63.5\mu\text{m}$ (center-to-center distance). Each pixel consists of a $56.4\mu\text{m} \times 200\mu\text{m}$ photodiode, an integration capacitor and a sample-and-hold circuit.

The integrated control logic makes operation very simple, with only a start and clock signal necessary. A third control input enables the integration period to be prematurely terminated at any time.

When the start signal is given hold mode is activated for all pixels simultaneously with the next rising clock edge; starting with pixel 1 the hold voltages are switched in sequence to the push-pull output amplifier. The second clock pulse deletes all integration capacitors and the integration period starts again in the background during the output phase. A run is complete after 128 clock pulses.

iC-LF is suitable for high clock rates of up to 5MHz. If this is not required the supply current can be reduced via the external bias setting.

CHIP LAYOUT



PAD DESCRIPTION

Name	Function
SI	Start Integration Input
CLK	Clock Input
AO	Analog Output (1mA push-pull)
VDD	+5V Supply Voltage (digital)
VCC	+5V Supply Voltage (analog)
RSET	Bias Current Adjust (by resistor from VCC; when linked to GND the internal bias setting is activated)
TP	Test Output
AGND	Analog Ground
GND	Digital Ground
DIS	Disable Integration Input (use is optional; input can be switched to GND or left open for compatibility with TSL1401)

External connections linking GND to AGND and VDD to VCC are required.

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.			Unit
					Min.	Max.	
G001	VDD	Digital Supply Voltage			-0.3	6	V
G002	VCC	Analog Supply Voltage			-0.3	6	V
G003	V()	Voltage at SI, CLK, DIS, RSET, TP, AO			-0.3	VCC+0.3	V
G004	I()	Current in RSET, TP, AO			-10	10	mA
E001	Vd()	ESD Susceptibility at all pins	MIL-STD-883, Method 3015, HBM 100pF/ 1.5kΩ			2	kV
TG1	Tj	Operating Junction Temperature			-40	125	°C
TG2	Tj	Storage Temperature Range	see package specification				

THERMAL DATA

Operating Conditions: VCC= VDD= 5V ±10%

Item	Symbol	Parameter	Conditions	Fig.				Unit
					Min.	Typ.	Max.	
T1	Ta	Operating Ambient Temperature Range (extended range on request)	see package specification					

OPTICAL CHARACTERISTICS: Diagrams

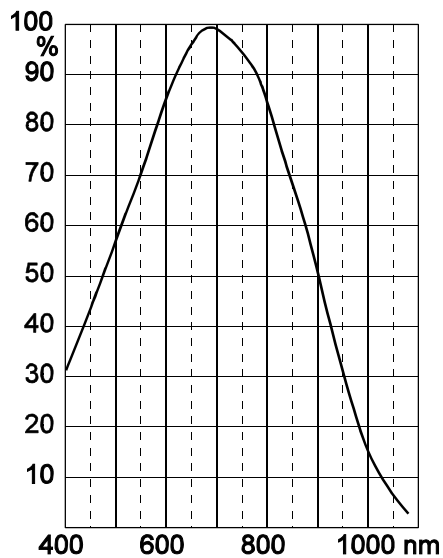


Fig. 1: relative spectral sensitivity

All voltages are referenced to ground unless otherwise noted.

All currents into the device pins are positive; all currents out of the device pins are negative.

OPERATING REQUIREMENTS: Logic

Operating Conditions: $V_{CC} = V_{DD} = 5V \pm 10\%$, $T_j = -25..85^\circ\text{C}$
 input levels $lo = 0..0.45V$, $hi = 2.4V..V_{CC}$, see Fig. 2 for reference levels

Item	Symbol	Parameter	Conditions	Fig.			Unit
					Min.	Max.	
I1	tset	Setup Time: SI stable before CLK lo-hi		2	50		ns
I2	thold	Hold Time: SI stable after CLK lo-hi		2	50		ns

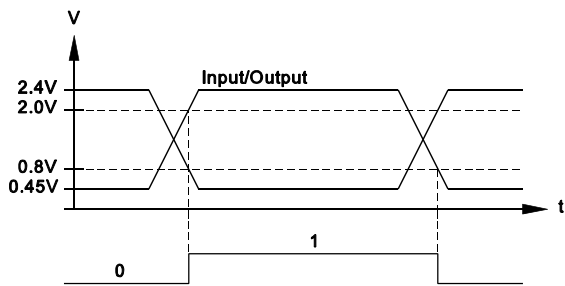


Fig. 2: reference levels

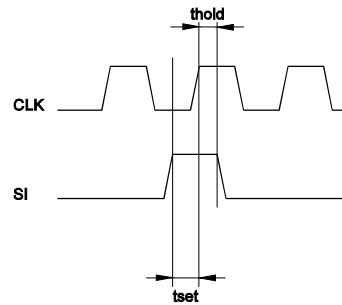


Fig. 3: timing diagram

DESCRIPTION OF FUNCTIONS

Normal operation

Following an internal power-on reset the integration and hold capacitances are deleted and the sample-and-hold circuit is set to sample mode. A high at SI and a rising edge at CLK triggers a readout cycle and with it a new integration cycle.

In this process the hold capacitances of pixels 1 to 127 are switched to hold mode immediately (SNH= 1), with pixel 128 (SNH128= 1) following suit one clock pulse later. This special procedure allows all pixels to be read out with just 128 clock pulses. The integration capacitances are deleted by a pulse-long reset signal (NRCI= 0) which occurs between the 2nd and 3rd falling edge of the readout clock pulse (see Figure 4). After the 127 pixels have been read out these are again set to sample mode (SNH= 0), likewise for pixel 128 one clock pulse later (SNH128= 0).

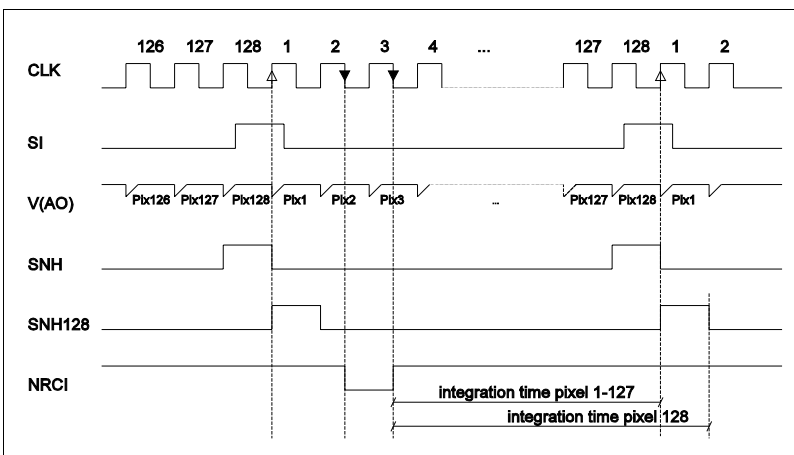


Fig. 4: readout cycle and integration sequence

If prior to the 128th clock pulse a high occurs at SI the present readout is halted and immediately reinitiated with pixel 1. In this instance the hold capacitances retain their old value i.e. hold mode prevails (SNH/SNH128= 0).

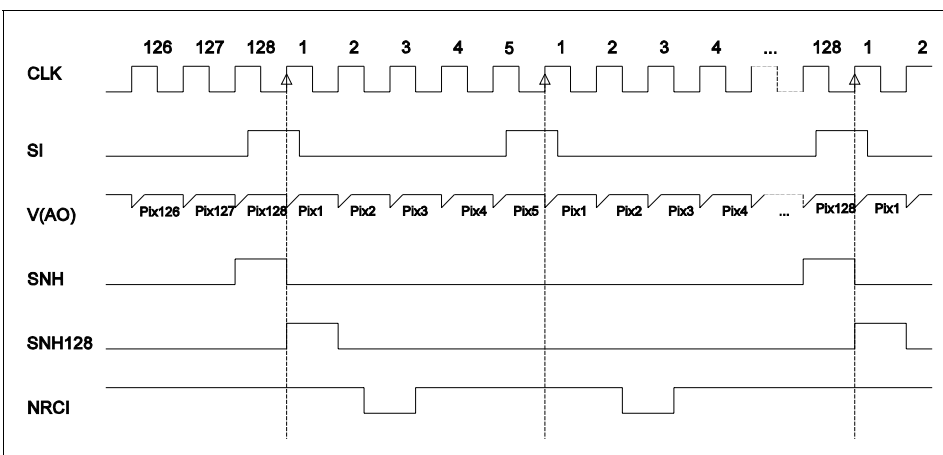


Fig. 5: restarting a readout cycle

If there are over 128 clock pulses until the next SI signal pixel 1 is output without entering hold mode; the output voltage tracks the voltage of the pixel 1 integration capacitance.

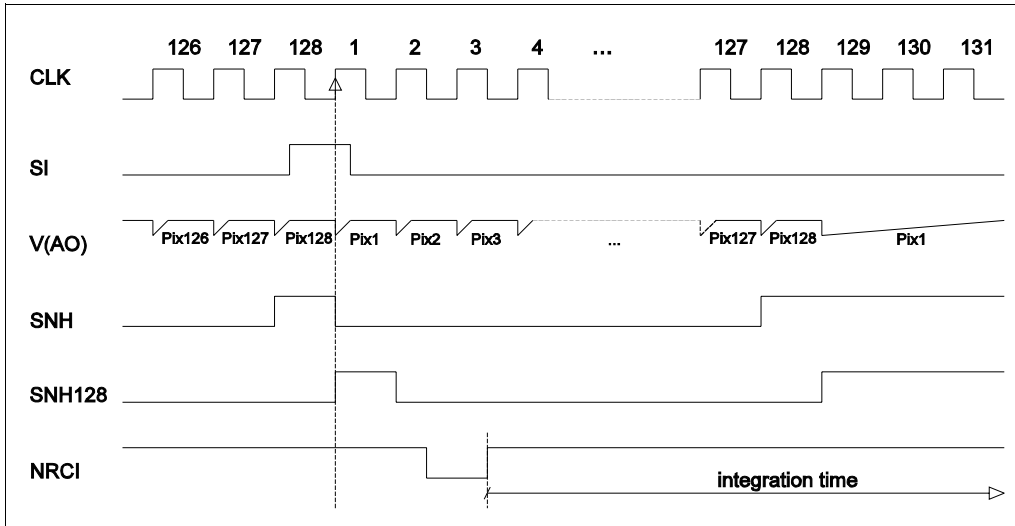


Fig. 6: clock pulse continued without giving a new integration start signal

Operation with the shutter function

Integration can be disabled at any time via pin DIS, i.e. the photodiodes are switched away from their corresponding integration capacitance when DIS is high and the current integration capacitance voltages are maintained. If this pin is open or switched to GND the pixel photocurrents are summed up by the integration capacitances until the next successive SI signal follows.

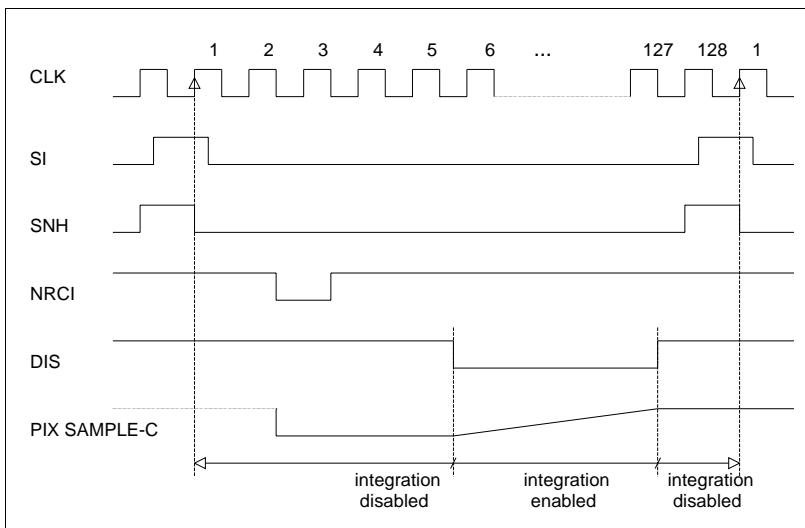


Fig. 7: defining the integration time via shutter input DIS

External bias current setting

In order to reduce the power consumption of the device an external reference current can be supplied to pin RSET what reduces the maximum readout frequency, however. To this end a resistor must be wired from VCC to RSET. If this pin is not used it should be linked to GND.

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ORDERING INFORMATION

Type	Package	Order designation
iC-LF	- OLGA	iC-LF chip iC-LF OLGA LF2C

For information about prices, terms of delivery, options for other case types, etc., please contact:

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