



CCD525 Time Delay Integration Line Scan Sensor

FEATURES

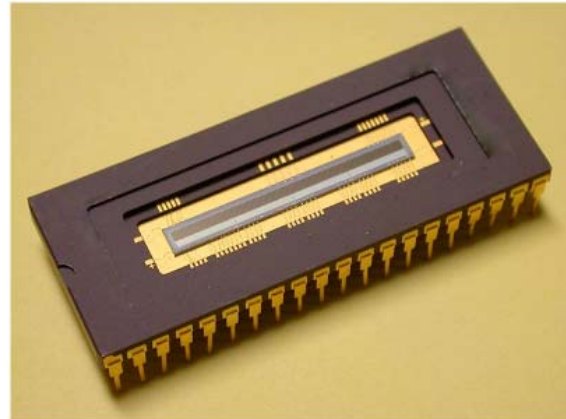
- 2048 Active Pixels Per Line
- 96 TDI Lines
- 13 μ m x13 μ m Pixels
- 4 High Speed Output Ports
- TDI Stages Selectable Between 96, 64, 48, 32, or 24
- 100 MHz Data Rate with 4 Outputs
Operating at 25 MHz
- 42 kHz Line Rate
- 2000X Antiblooming Protection
- High Sensitivity
- RoHS Compliant

GENERAL DESCRIPTION

The CCD525 is a Time Delay Integration (TDI) sensor designed for a wide range of imaging applications requiring high speed operation combined with high sensitivity. The sensor is capable of producing a total data rate of 100 MHz (line rate > 42 kHz). The CCD has a total imaging area of 2048 contiguous elements by 96 TDI rows. The pixel dimensions are 13 μ m by 13 μ m. The CCD overall dimensions are 27.940 mm x 3.302 mm. The sensor is mounted in a custom 40-pin dual-in-line ceramic package.

The CCD525 imaging area is controlled by 3-phase timing, and exposure control is performed by selecting the number of active TDI stages. Independent TDI control gates allow the following number of TDI stages to be selected: 96, 64, 48, 32, or 24. The CCD525 features lateral anti-blooming structures capable of 2000X over-saturation protection.

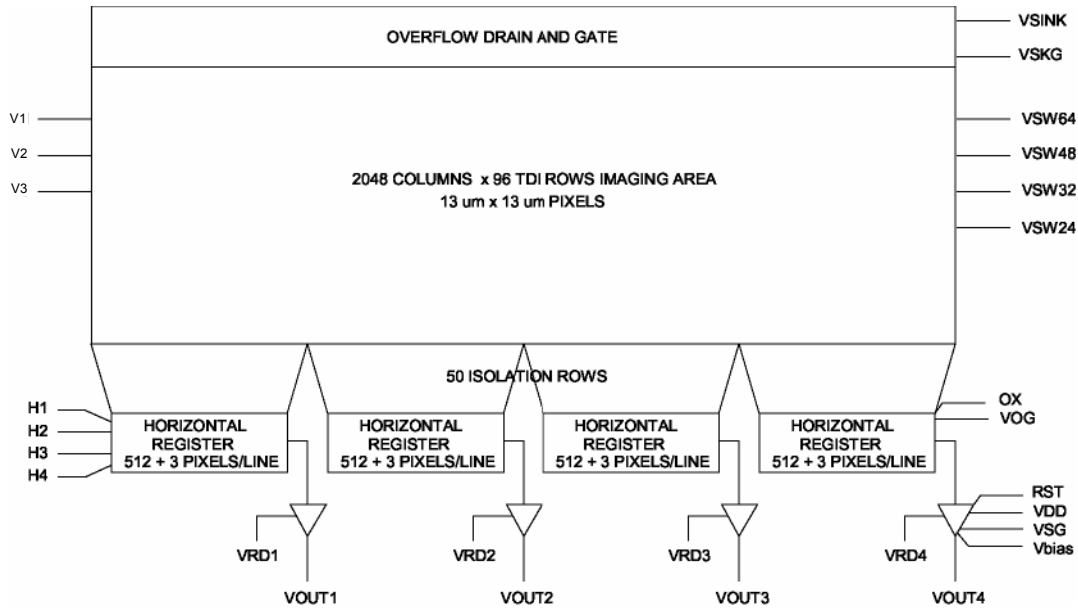
The vertical (parallel) imaging register is separated from the horizontal (serial) registers by 50 isolation rows. The isolation rows are also controlled by 3-phase timing. The isolation rows are covered with a light shield and are used to transfer the charge from the imaging area to four horizontal registers. The horizontal registers are controlled by 4-phase timing. The design of the horizontal registers has been optimized for high charge transfer efficiency at low signal levels.



Each horizontal register is connected to a high speed output amplifier. The output amplifier is a three-stage source follower designed for high conversion gain and extended bandwidth.

DEVICE ARCHITECTURE

The CCD525 operates in buried channel mode for optimal performance. The imaging area consists of 2048 contiguous pixels by 96 rows. Photogenerated charge is integrated in this region, then following the integration time, the charge is transferred line by line to the adjacent isolation rows for readout. The number of active TDI rows is simply controlled by biasing the appropriate control gates, VSWxx, low. Normal vertical timing is employed across the array irrespective of the selected number of active TDI stages. The last gate in the vertical register is also called the vertical transfer gate, ΦX . The charge is transferred from the vertical register to the horizontal registers when ΦX is clocked low. The horizontal registers require 4-phase timing. Charge is transferred, pixel by pixel, to the floating diffusion sense node where it produces a voltage change corresponding to the signal level. After the signal is sampled, the reset gate is clocked high to clear the signal, and restore the potential of the sense node to the VRD reset drain voltage. There are 3 prescan elements in each video line.

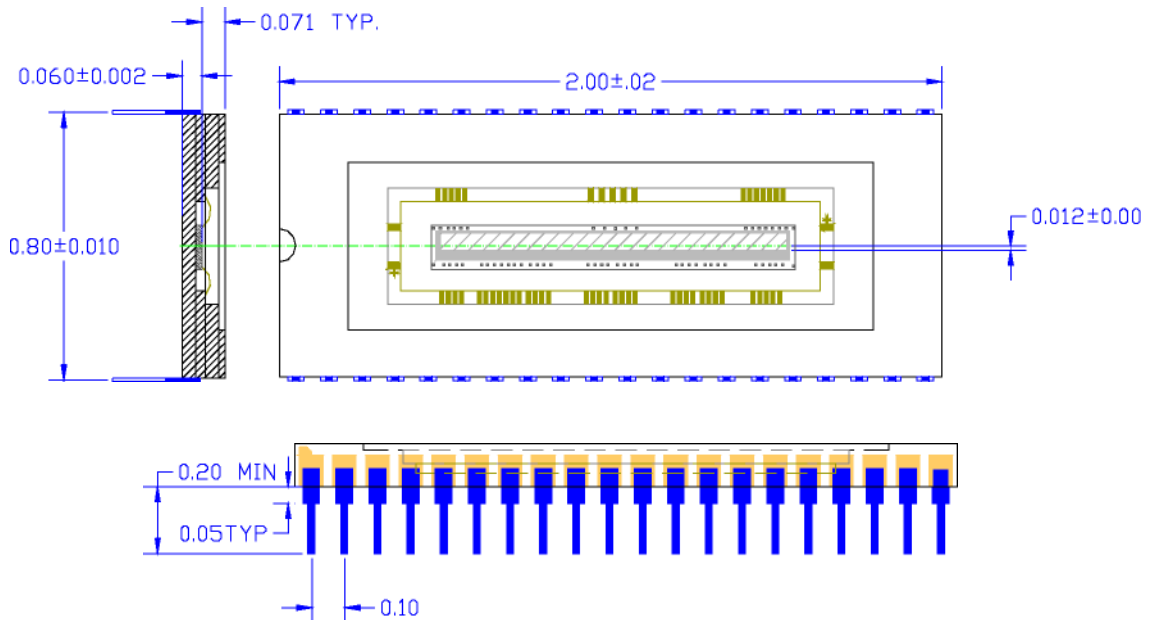


CCD525 Block Diagram

PACKAGE INFORMATION

The CCD525 is mounted in a ceramic dual-in-line package with 40 pins. The spacing between each pin is 0.100", and the distance between the

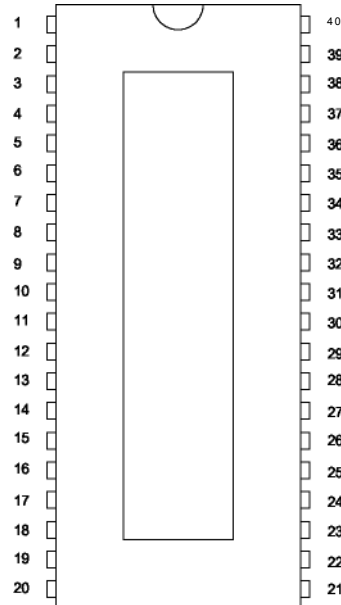
two rows of pins is 0.800". The overall dimensions of the package are 2.000" x 0.810" x 0.130". The package window is covered with an antireflection (AR) coated cover glass.



CCD525 Package Drawing

PACKAGE PIN ASSIGNMENT

CCD525 Package
pinout diagram
(TOP VIEW)



PIN NAME AND DESCRIPTION

Pin	Pin Name	Description	Pin	Pin Name	Description
1	ΦR	Reset gate	40	H3	Horizontal CCD clock phase 3
2	VSS	Substrate	39	H1	Horizontal CCD clock phase 1
3	N/C	No connect	38	H2	Horizontal CCD clock phase 2
4	VRD1	Output 1 reset drain	37	H4	Horizontal CCD clock phase 4
5	VDD	Amplifier supply	36	ΦX	Vertical transfer gate
6	Vout1	Video output 1	35	VLS	Light shield ground
7	VOG	Output gate	34	V1	Vertical CCD clock phase 1
8	N/C	No connect	33	N/C	No connect
9	VRD2	Output 2 reset drain	32	VSW24	TDI 24 select gate
10	N/C	No connect	31	V2	Vertical CCD clock phase 2
11	Vout2	Video output 2	30	VSW32	TDI 32 select gate
12	VSG	Amplifier supply return	29	VSW48	TDI 48 select gate
13	Vbias	Current source bias	28	V3	Vertical CCD clock phase 3
14	N/C	No connect	27	VSW64	TDI 64 select gate
15	VRD3	Output 3 reset drain	26	N/C	No connect
16	Vout3	Video output 3	25	VSKG	Overflow gate bias
17	VDD	Amplifier supply	24	Vsink	Overflow drain bias
18	N/C	No connect	23	ΦX	Vertical transfer gate
19	VRD4	Output 4 reset drain	22	ΦR	Reset clock
20	Vout4	Video output 4	21	VSS	Substrate

ABSOLUTE MAXIMUM RATINGS

Description	Min	Max	Units	Remarks
Diode voltages	0	28	V	Pins VRD, VDD, VSS, Vout, Vsink
CCD gate voltages	-16	16	V	Pins V1, V2, V3, H1, H2, H3, H4
Single gate voltages	-5	16	V	Pins Φ R, Φ X, VOG, VSKG
Gate-to-gate voltages		16	V	
Storage temperature	-50	+65	°C	
Humidity	30	80	%RH	

DC OPERATING CHARACTERISTICS

Pin Name	Description	Min	Typical	Max	Units & Tolerance
VDD	Amplifier supply	+13.5	+14	+14.5	V \pm 5%
VSG	Amplifier supply return	+0.5	+0.7	+0.9	V \pm 5%
Vbias	Current source bias	+1.5	+2	+2.5	V \pm 5%
VRD	Output reset drain	+10	+10.5	+11	V \pm 5%
VOG	Output gate	+0.5	+1	+1.5	V \pm 5%
VSS	Substrate	0	0	0	V \pm 5%
VLS	Light shield voltage	0	0	0	V \pm 10%
Vsink	Overflow drain bias	+13.5	+14	+14.5	V \pm 10%
VSKG	Overflow gate bias	-2.5	-2	-1.5	V \pm 10%
VSWxx	TDI select gate (xx=24, 32, 48, 64)	-6.5	-6	-5.5	V \pm 5%

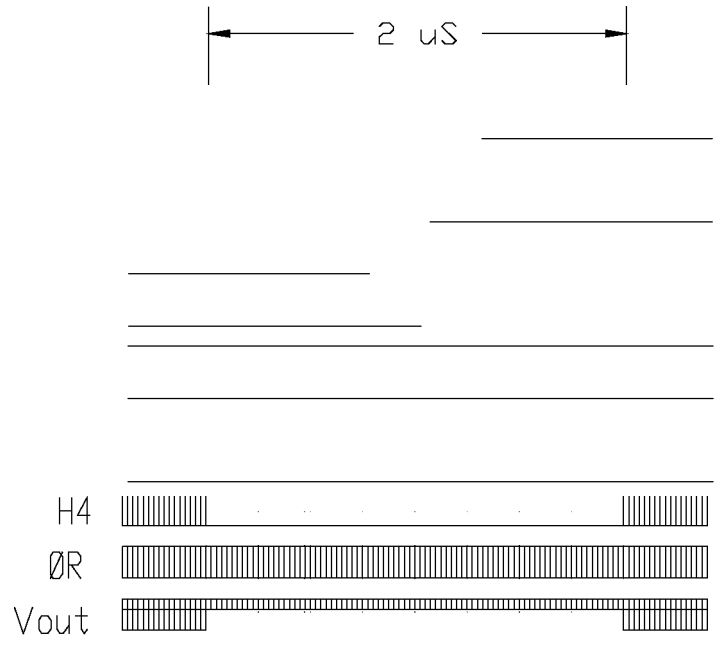
AC OPERATING CHARACTERISTICS

Pin Name	Description	Level	Min	Typical	Max	Units & Tolerance
V1, V2, V3	Vertical CCD gate	Low	-1	0	0	V \pm 10%
		High	+9.5	+10	+10.5	V \pm 10%
H1, H2, H3, H4	Horizontal CCD gate	Low	-1	0	0	V \pm 10%
		High	+5.5	+6	+6.5	V \pm 10%
Φ R	Reset gate	Low	+0.5	+1	+1	V \pm 10%
		High	+8.5	+9	+9.5	V \pm 10%
Φ X	Vertical transfer gate	Low	-1	0	0	V \pm 10%
		High	+9.5	+10	+10.5	V \pm 10%
VSWxx	TDI select gate (xx=24, 32, 48, 64)	Low	-1	0	0	V \pm 10%
		High	+9.5	+10	+10.5	V \pm 10%
IDD	Amplifier current per output		5	7	9	mA

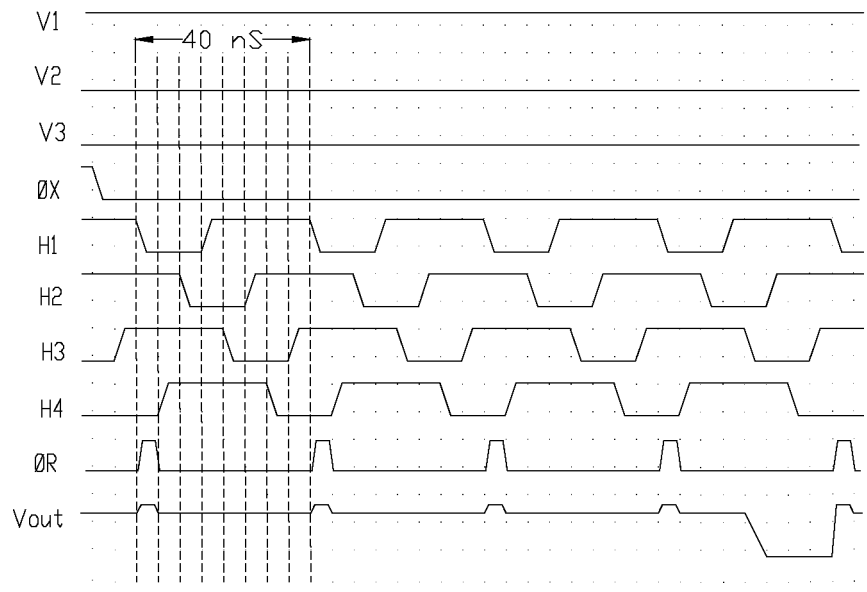
GATE CAPACITANCE

Pin Name	Description	Effective Capacitance	Remarks
V1, V2, V3	Vertical CCD gate	3900 pF	Per phase
H1, H2, H3, H4	Horizontal CCD gate	220 pF	Per phase
Φ R	Reset gate	42 pF	Per gate
Φ X	Vertical transfer gate	67 pF	Per gate
VSWxx	TDI select gate (xx=24, 32, 48, 64)	140 pF	Per gate

CCD CLOCK TIMING



CCD525 Vertical Clock Timing



CCD525 Horizontal Clock Timing

PERFORMANCE SPECIFICATIONS

Description	Symbol	Min	Typical	Max	Units	Remarks
Vertical saturation charge	Qsat	150	200	-	Ke-	
QE at 650 nm	QE	20	22	-	%	
Readout noise	Noise	-	70	100	e-	
Dynamic range	DR	2700	3000	-		
Horizontal CTE	HCTE	0.99993	0.99995	-		Per transfer
Vertical CTE	VCTE	0.99995	0.99999	-		Per transfer
Photoresponse non-uniformity	PRNU	-	5	10	%	
Dark current	Idark	-	1	-	nA/cm ²	
Dark signal charge density	Idark	-	10500	-	Elec/pixel /sec	
Dark signal non-uniformity	DSNU	-	< 5%	-	Qsat	
Output amplifier DC offset		-	10.3	-	Vdc	
Output amplifier sensitivity		2.5	3	3.5	μV/e-	
Antiblooming	AB	1500	2000	-		X saturation
Peak responsivity	Resp.	-	320	-	V/μj/cm ²	At 650 nm
Test conditions						
1. Tests were performed at 25°C with horizontal clock frequency of 25 MHz per output and vertical clock frequency of 42 kHz.						

CCD HANDLING

CCD sensors are very sensitive to ESD damage, therefore, strict static-safe handling precautions must be carefully observed during their use. Evidence of ESD damage resulting from improper handling may invalidate the warranty.

- The work station and the operator must be fully grounded when the CCD is removed from its shorting bars or conductive foam.
- The receiving socket and associated circuitry must be adequately grounded.
- The CCD must be stored with proper shorting bars attached or mounted in conductive foam

WARRANTY

Within twelve months of delivery to the end customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging product if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Imaging certifies that its products are fully inspected and tested at the factory prior to shipment and that they conform to the stated specifications.

This product is designed, manufactured, and distributed utilizing the ISO 9000:2000 Business Management System.

Fairchild Imaging
1801 McCarthy Blvd., Milpitas, CA 95035
(800) 325-6975, (408) 433-2500
Internet: www.fairchildimaging.com

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