



## ***CAM8525 Characteristics*** ***Camera Array Board***

### ***Features***

- Array board size: 4" x 6" (see Figures 1 and 2)
- Time delay integration operation
- Anti-blooming, typically >50x saturation charge
- 2048 horizontal pixels, 13 $\mu$ m SQ
- 24, 32, 48, 64, 96 selectable TDI stages
- CCD signal processing with quad AD9840 monolithic chips
- 4 Synchronous Output Ports
- 8-bit digital data out (LVTH)\*
- Remote gain and offset control for each output (4x)
- Separate connectors for power and control data lines (see Figure 1)

### ***Description***

TDI sensor with manually selectable number of TDI stages for user control of sensitivity. Array driver board provides bias voltages, ISP programmable timing and driver clocks to the CCD sensor. Four CCD monolithic signal processing chips include buffer amps and CDS (correlated double sampling) circuitry and an A/D converters providing digital outputs.

### ***Sensor***

- 2048 x 96 pixels
- 13x13  $\mu$ m pixel dimension
- 4 output taps

### ***Electrical Interface Connections (see Figure 2)***

Power connector (see Figure 8, J4):

- 15  $\pm$  0.45V, 200ma, ripple 50mvpp
- 5  $\pm$  0.25V, 550ma, ripple 50mvpp

Two digital data IDC high density connectors (see Figure 5, J1 and Figure 6, J2)

Serial Interface ISP connector (see Figure 7, JP3)

***\* Low voltage logic levels: high = 3V, low = 0V***

### ***Input Data and Control Signals***

SYNC\_IN, synchronizes start of line transfer to moving object

- Rising edge starts line transfer
- Falling edge occurs at least 100ns after rising edge

RESET\_IN, resets all video processors on array board (active low)

Manually selectable TDI stages (24, 32, 48, 64 or 96)

S\_DATA\_IN, serial data input for gain and offset control

S\_CLOCK\_IN, clocks serial data input valid on positive edge and serial data output valid on negative edge

S\_LOAD, enables S\_CLOCK\_IN

### ***Output Signals***

LVAL\_OUT, output line data valid (active high)

STROBE\_OUT, output pixel data valid on falling edge of strobe

Digitized data output, 8 bits per pixel per channel, 4 channels total

S\_DATA\_OUT, serial data output for gain and offset

### ***Performance Specs (96 TDI Stages)***

Per channel data rate	22.5MHz
Line rate	40KHz
Saturation output amplitude	255 DN max
Photoresponse non-uniformity (@ 128 DN average signal level)	25 DN max
RMS noise (@ amplifier gain of 4)	1 DN max
Responsivity (@ peak wavelength)	196 DN / nj cm <sup>-2</sup>

CCD525/Array Board Assembly

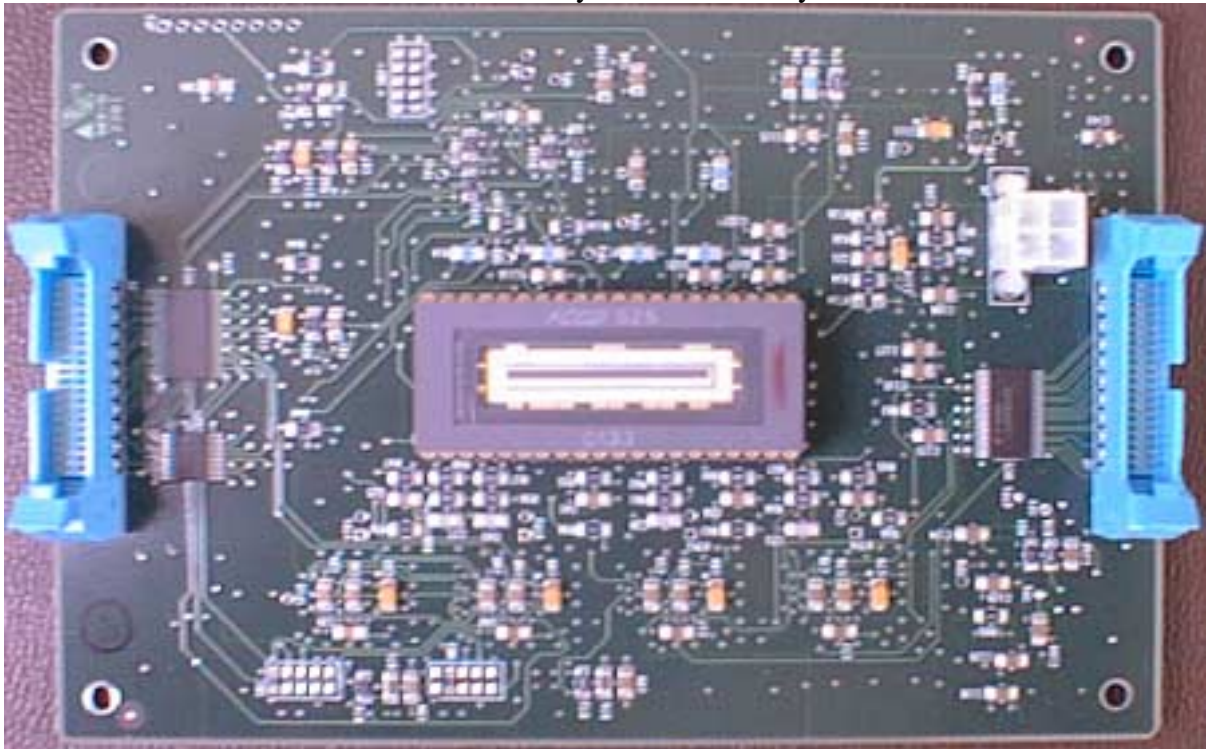


Figure 1 Board Top View

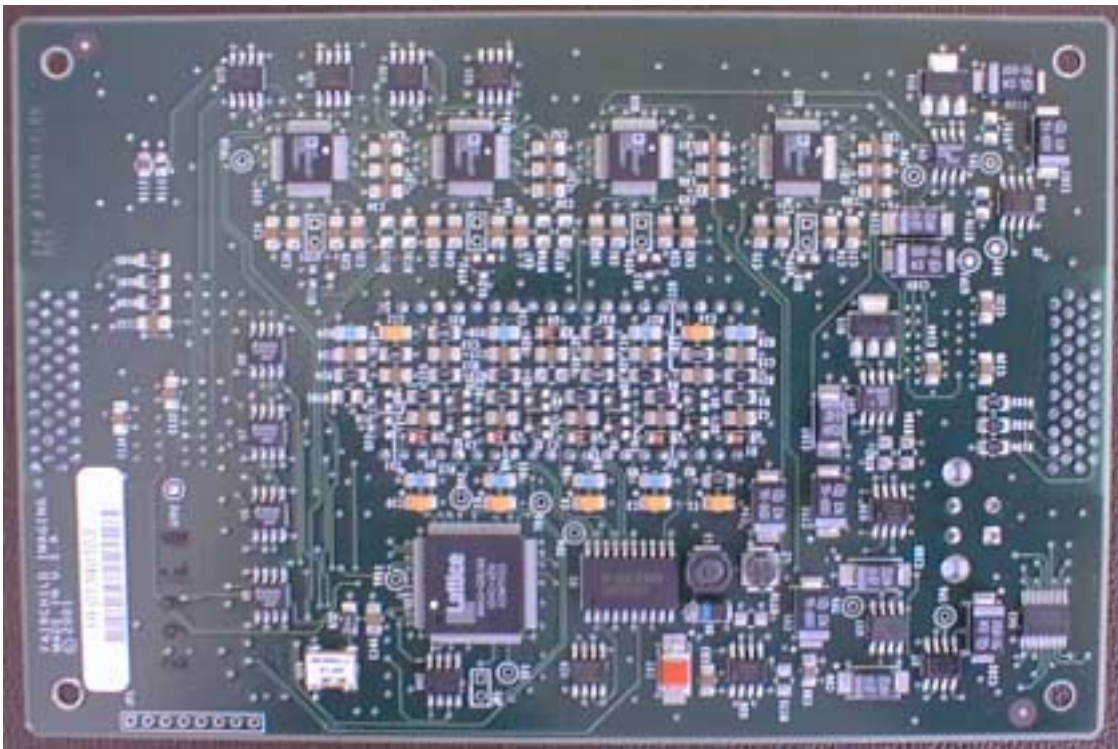


Figure 2 Board Bottom View

Array Board Assembly Drawings with Connector Locations

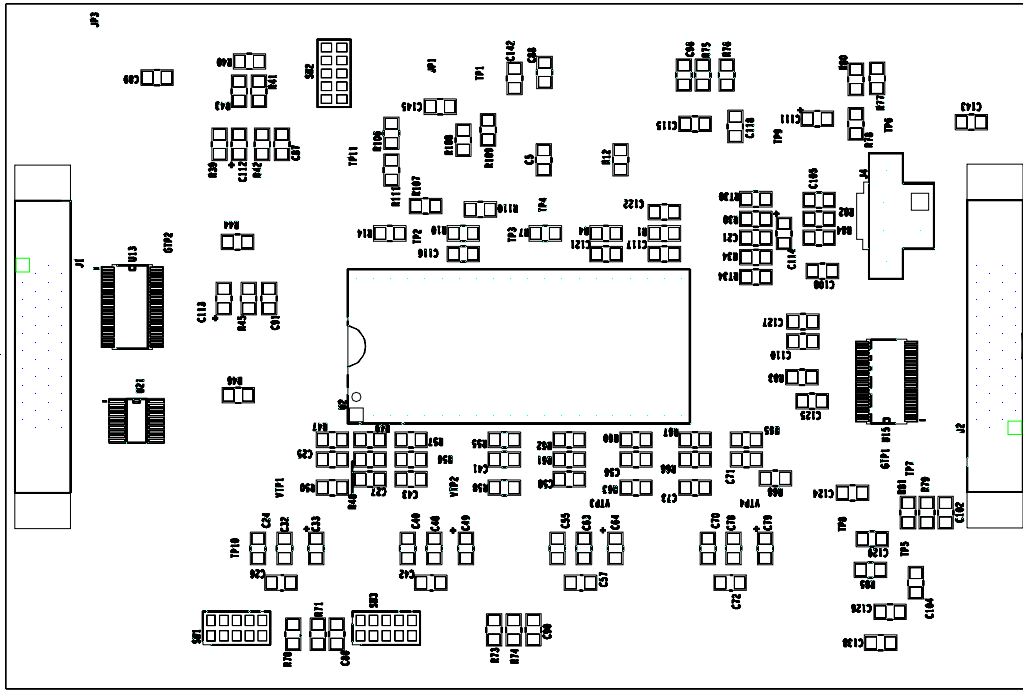


Figure 3 Top View

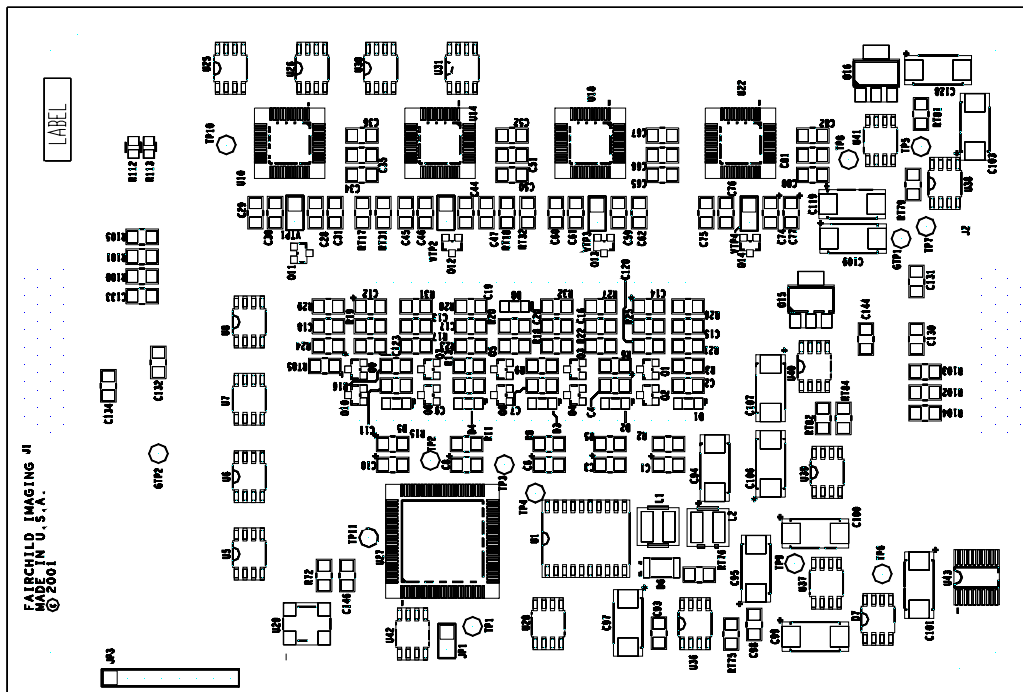


Figure 4 Bottom View

**FIGURE 5****J1—40 Pin High Density IDC Connector**

<i>Pin</i>	<i>Signal</i>	<i>Pin</i>	<i>Signal</i>
1	VD10	2	GND
3	VD11	4	GND
5	VD12	6	GND
7	VD13	8	GND
9	VD14	10	GND
11	VD15	12	GND
13	VD16	14	GND
15	VD17	16	GND
17	VD20	18	GND
19	VD21	20	GND
21	VD22	22	GND
23	VD23	24	GND
25	VD24	26	GND
27	VD25	28	GND
29	VD26	30	GND
31	VD27	32	GND
33	LVAL_OUT	34	GND
35	STROBE_OUT	36	GND
37	SYNC_IN	38	GP1_IN
39	RESET_IN	40	GND

**FIGURE 6****J2—40 Pin High Density IDC Connector**

<i>Pin</i>	<i>Signal</i>	<i>Pin</i>	<i>Signal</i>
1	VD30	2	GND
3	VD31	4	GND
5	VD32	6	GND
7	VD33	8	GND
9	VD34	10	GND
11	VD35	12	GND
13	VD36	14	GND
15	VD37	16	GND
17	VD40	18	GND
19	VD41	20	GND
21	VD42	22	GND
23	VD43	24	GND
25	VD44	26	GND
27	VD45	28	GND
29	VD46	30	GND
31	VD47	32	GND
33	S_DATA_OUT	34	GND
35	GPOUT	36	GND
37	S_DATA_IN	38	S_CLK
39	S_LOAD	40	NOT CONNECTED (NC)

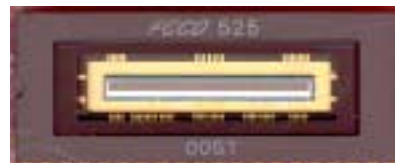
**FIGURE 7****JP3—ISP 8 Pins In-Line Header**

<i>Pin</i>	<i>Description</i>
1	+3.3V
2	S_DATA_OUT (TDO)
3	S_DATA_IN (TDI)
4	In System Program Enable (active low)
5	Not Connected (NC)
6	Mode (TMS)
7	Ground
8	S_CLOCK (TCK)

**FIGURE 8****J4—Power Connector**

<i>Pin</i>	<i>Description</i>
1	No Connection (NC)
2	+5 Volts
3	+15 Volts
4	Return (GND)

**CCD525**  
**2K x 96 Element**  
**TDI – Time, Delay and Integration Sensor**



**Features**

- 2048 pixels per line
- 96 lines of integration
- 13 $\mu$ m x 13 $\mu$ m pixel size
- # of TDI stages selectable from 96, 64, 48, 32 or 24
- 4 outputs – each capable of 25MHz data rate – 100MHz total data rate
- Horizontal antiblooming
- High responsivity

***Description***

The CCD525 is a 2K (2048) pixel x 96 line, high speed TDI sensor. With four outputs, each running at 25MHz, the CCD525 can provide a total data rate of 100MHz enabling the CCD to run at better than 44KHz line rate. Utilizing Lockheed Martin Fairchild System's proprietary buried channel CCD process, the CCD525 achieves consistent, superior TDI performance.

The active imaging area is organized as 2048 vertical columns and 96 horizontal TDI rows. The exposure level can be controlled by reducing the number of TDI rows to 64, 48, 32 or 24 through the use of the user-selectable TDI switch gates. The CCD525 also provides a horizontal antiblooming structure which provides 100X oversaturation protection. Even though this structure produces a fill factor of less than 100%, it has much higher quantum efficiency (QE) than other antiblooming structures. Therefore, the effective quantum efficiency (fill factor X QE) remains higher than these other competing structures.

The active imaging area is separated from the 4 horizontal output registers by 50 isolation rows. These isolation rows are covered by a metal light shield to protect them while charge transfers to the output registers. Both the active imaging area and the isolation region utilize 3-phase clocking.

The 4 horizontal output registers utilize 4-phase clocking. Special design techniques have been implemented to maximize charge transfer efficiency especially at low light levels. The output amplifier is a 3-stage source follower configuration. This allows maximum scale factor (charge to voltage conversion) and maximum bandwidth.

The CCD525 is housed in a standard 40 pin (100 mil pin spacing) ceramic DIP package. It has an AR coated window.

**Performance Specifications**

Test conditions;  
 Fdata = 25MHz per output  
 Fline = 44KHz  
 Temp = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Units
Vsat	Saturation Voltage	400	550		mV
Qsat	Saturation Charge		150		Ke-
SF	Scale Factor	2.5	3.5		μV/e-
Noise	Noise (rms)		.2	.4	mV
DR	Dynamic Range	1000	2750		
HCTE	Horizontal CTE	0.99992	0.99995		per transfer
VCTE	Vertical CTE	0.99995	0.99999		per transfer
PRNU	Photoresponse Non-Uniformity		5	10	%
AB	Antiblooming Capacity	500	2000		x oversat.

**CCD525  
 BLOCK DIAGRAM**

