

Preliminary

Linear Image Sensor

Product Name

C212

Approval		Notes		
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All specifications of this device are subject to change without notice.				

Revision control sheet

Rev	Date	From	Description
A	Dec. 2, 2003		Change drawing pin name

C212

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Introduction

1. Features:

- 522 image sensing elements
- 21.15 um pixel to pixel spacing
- 400 dpi resolution with color filter on the horizontal direction
- 1200 dpi resolution without color filter on the horizontal direction
- 42 um pixel length (600 dpi resolution on the vertical direction)
- 400 or 1200 dpi resolution
- Black & white or color version
- Ultra-High speed clock rate ~ 25 MHz
- Ultra-high pixel readout rate ~ 75 M pixel / second
- Three video outputs simultaneously (one output for each Red, Green and Blue color)
- Suitable for either CCFL or LED light source
- Low noise
- Very good Linearity, equal to or close to one
- Low power consumption
- On chip dual correlated double sampling (CDS) circuitry
- On chip timing generator and clock driver

2. Description:

C212 linear image sensor is designed for high speed, color digital copier application. The sensor was formed by a series of 522 photo diodes with 21.15 um pixel to pixel spacing. Three (red, green and blue) color filters alternately deposited on the photo diode area to form a 400 dpi resolution of color sensor chip. Three video outputs readout each color of the video signal simultaneously. The scan speed is increased by three times since each video signal only reads about one third of the photo detectors. A proprietary dual correlated double sampling (CDS) circuitry is used to cancel reset noise and reduce fixed pattern noise. This chip also has build in on chip power down circuitry to reduce power consumption. The photo diodes are parallel dump and serial readout devices. The device is easily operated with a start pulse, a clock pulse, and a 5 V and Vref power supply. The C212 sensor chip without color filter option is also available.

The device is designed for the application of silicon butting contact image sensors. The length of the chip is about 11.03 mm. One chip can be butted to another chip to form a long image sensor module. The length of the module can be extended to A6, A4, B4, A3, ... up to A0 size. For silicon butting CIS application, the End of Pulse (EP) of the first chip is connected to the Start Pulse (SP) of the next chip. This device can be used in a wide variety of applications such as color high speed scanner, digital copier, mark reader, bar code reader, OCR, edge detector, positioning and optical encoding, etc.

Terminal Description

No	Symbol	I/O	Description
1	SP	I	Start pulse input
2	DP	O	Delay pulse output
3	IP	I	Input pulse
4	CP	I	Clock pulse input
5	DVDD	I	Logic power supply; 5 V
6	DGND	I	Logic ground
7	VREF	I	Reference voltage for OP amp; 2.5 V
8	BG	O	Bandgap voltage output
9	AGND	I	Analog ground
10	AVDD	I	Analog power supply; 5 V
11	Vout (B)	O	Blue color analog output signal
12	Vout (G)	O	Green color analog output signal
13	Vout (R)	O	Red color analog output signal
14	EP	O	End of pulse output

Table 1. Terminal Description

Functional block diagram:

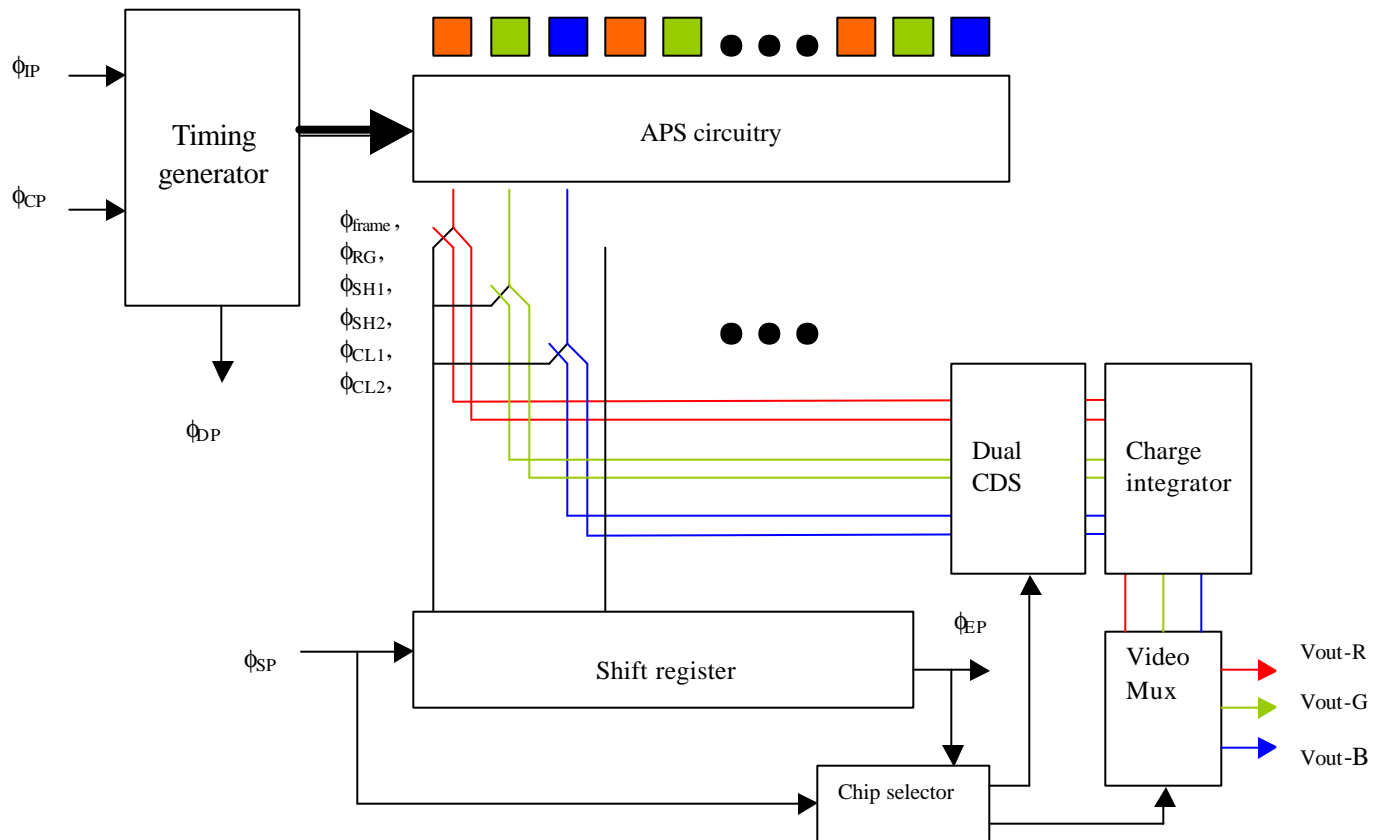


Figure 1. Functional Block Diagram

Bonding Pad Layout Diagram

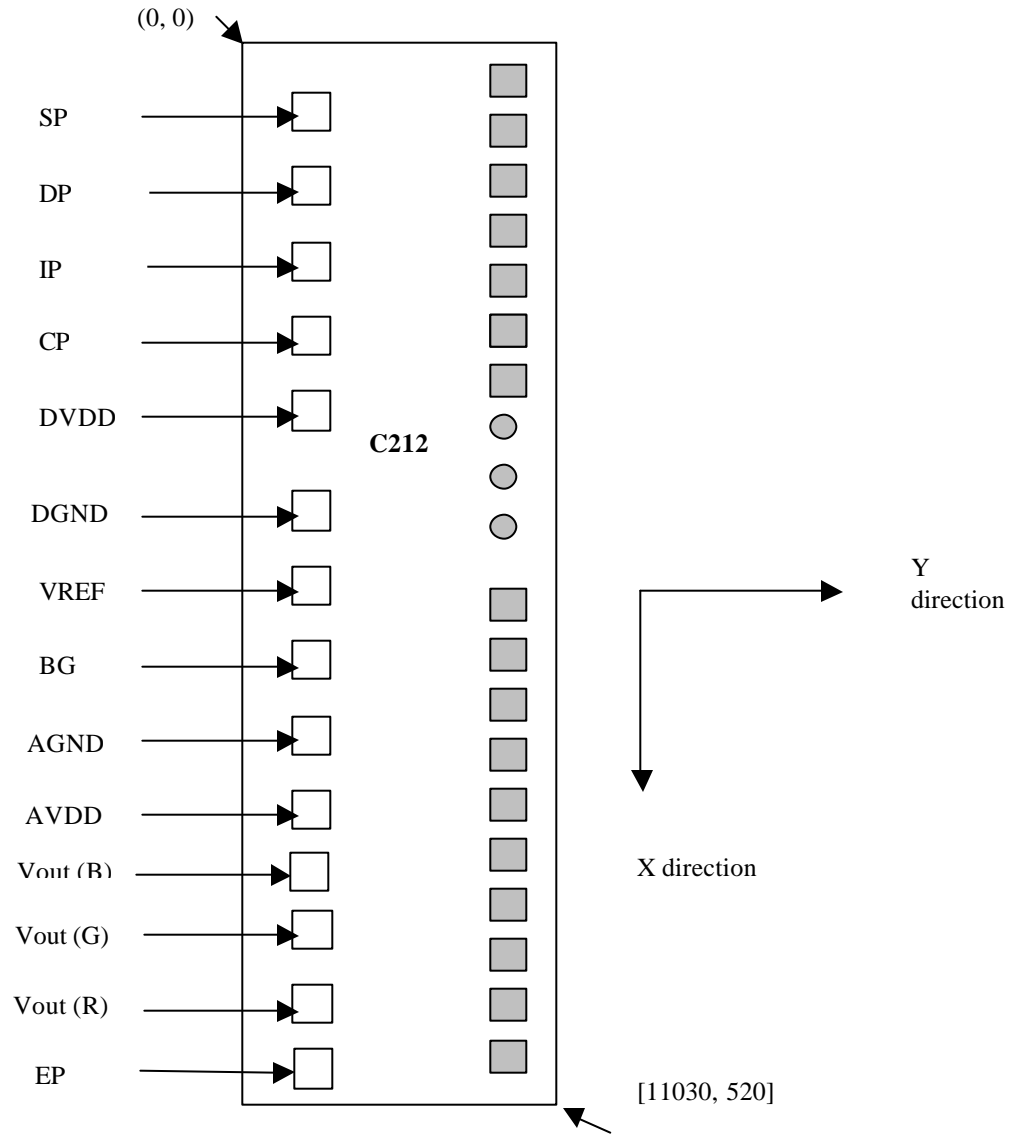


Figure 2. Bonding pad layout diagram

Bonding Pad Description

Pin #	Symbol	Location (x , y) in unit of mm	Description
1	SP	(682, 70)	Start pulse input
2	DP	(1022, 70)	Delay pulse output
3	IP	(4261, 70)	Input pulse
4	CP	(5094, 70)	Clock pulse input
5	DVDD	(5328, 70)	Logic power supply; 5 V
6	DGND	(5858, 70)	Logic ground
7	VREF	(6379, 70)	Reference voltage input; 2.5 V
8	BG	(6599, 70)	Bandgap voltage output
9	AGND	(6973, 70)	Analog ground
10	AVDD	(7473, 70)	Analog power supply; 5 V
11	Vout (B)	(8242, 70)	Blue color output signal
12	Vout (G)	(9042, 70)	Green color output signal
13	Vout (R)	(9842, 70)	Red color output signal
14	EP	(10546, 70)	End of pulse output

Table 2. Bonding pad description

Note: Origin: (0 μm , 0 μm) at the left corner of the chip.
 Location: (x μm , y μm) is measured at the center of the pad.
 Pad size: (125 μm by 80 μm)
 Chip size: 520 μm by 11030 μm for the chip without scribe line.
 600 μm by 11110 μm with scribe lines.

Electro-Optical Characteristics

Test conditions:

Measured at $\phi_{\text{CP}} = 1 \text{ MHz}$, $V_{\text{dd}} = 5\text{V}$, $t_{\text{int}}^{*(1)} = 4 \text{ ms}$, $\lambda^{*(2)} = 565 \text{ nm}$, $\text{Gain}^{*(4)} = 1$,
 $T_{\text{A}}^{*(5)} = 25 \text{ }^\circ\text{C}$, light intensity = 12 LUX.

[See readout circuitry (unless otherwise noted).]

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
	Sensitivity (without color filter)			35		V/lux s
	Sensitivity (R)			30		V/lux s
	Sensitivity (G)			28		V/lux s
	Sensitivity (B)			15		V/lux s
	Total active pixels			522		Pixels
	Red color pixels			174		Pixels
	Green color pixels			174		Pixels
	Blue color pixels			174		Pixels
V_{ref}	Reference voltage			2.5		V

f_{clk}	Clock frequency			12	25	MHz
f_{px}	Pixel rate			36	75	MHz
V_n	Random noise			2		mVrms
$V_c^{*(6)}$	Compensated analog output voltage (without color filter)	Light on		1.5	2	V
	(R)			1.5	2	V
	(G)			1.5	2	V
	(B)			0.75	1	V
$U_c^{*(7)}$	Compensated non-uniformity	Pixel 2 ~ 173**, within a chip	-20	---	+20	%
$U_{p_5pix}^{*(8)}$	8 pixel white level non-uniformity	Every 8 pixels, within a chip	-10	---	10	%
$U_{cadj}^{*(9)}$	Compensated adjacent pixel non-uniformity	Within a chip	-15	---	15	%
$C_c^{*(10)}$	Chip-chip compensated non-uniformity	Within a wafer	-20	---	+20	%
$V_d^{*(11)}$	Analog output voltage at dark level	Light off			45	mV
$U_d^{*(12)}$	Dark signal non-uniformity	Within a chip			20	mV
$C_d^{*(13)}$	Chip-chip dark signal non-uniformity	Within a wafer	---	---	20	mV
	Image lag			0		%

Table 3. Electro-Optical characteristics

Definition:

- t_{int} is the integration time. It is equal to the interval between two start pulses.
- λ is the wavelength of the light source.
- C_{ext} is the off-chip load capacitance for I_{out} .
- Gain is the gain of an off-chip video operation amplifier.
- TA is the ambient temperature.
- $V_c = (V_{cmax} + V_{cmin}) / 2$
where V_{cmax} is the maximum compensated voltage of the whole array.
 V_{cmin} is the minimum compensated voltage of the whole array.
- U_c is the pixel-to-pixel compensated photo response non-uniformity within a chip.
 $U_c = [((V_{cmax} - V_{cmin})/2) / V_c] \times 100\%$
- $U_{p_8pix} = \text{Max} \{ \text{Max} [V_p(i), V_p(i+1), \dots, V_p(i+7)] - \text{Min} [V_p(i), V_p(i+1), \dots, V_p(i+7)] \} / \{ \text{Max} [V_p(i), V_p(i+1), \dots, V_p(i+7)] + \text{Min} [V_p(i), V_p(i+1), \dots, V_p(i+7)] \}$
($i = 1, 2, \dots, 60$)
where $V_p(i)$ is the video signal output of a pixel # i
 $V_p(i+1)$ is the video signal output of a pixel # $(i+1)$
:
:
 $V_p(i+7)$ is the video signal output of a pixel # $(i+7)$
- $U_{cadj} = \text{Max} [|V_c(i) - V_c(i+1)| / V_c(i)] \times 100\%$, ($i = 2, 3, \dots, 343$)
where $V_c(i)$ is the compensated video signal output of a pixel # i
 $V_c(i+1)$ is the compensated video signal output of a pixel # $(i+1)$
- C_c is the chip-to-chip compensated photo response non-uniformity within a wafer

$$C_c = [(V_c - V_{cavg}) / V_{cavg}] \times 100\%$$

where V_{cavg} is the average compensated output signal of all chips within a wafer

11. $V_d = (V_{dmax} + V_{dmin}) / 2$

where V_{dmax} is the maximum dark voltage of the whole array.

V_{dmin} is the minimum dark voltage of the whole array.

12. $U_d = V_{dmax} - V_{dmin}$

13. C_d is the chip-to-chip dark voltage non-uniformity within a wafer.

$$C_d = V_d - V_{davg}$$

where V_{davg} is the average dark voltage of all chips within a wafer.

** Pixel # 1 and # 174 measured by U_{p_8pix}

Absolute maximum ratings:

Power supply voltage, V_{DD}	7 V
Power supply current, I_{DD}	60 mA
Digital input voltage range, V_{ih}	V_{DD}
Digital input current range, I_{ih}	-20 mA to 20 mA
Operating free-air temperature range, T_A	0 °C ~ 50 °C
Storage temperature range, T_{stg}	25 °C ~ 70 °C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended operating conditions:

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.5	5	5.5	V
Power supply current	I_{DD}		3.5		mA
Input voltage	V_i			V_{DD}	V
High level input voltage	V_{ih}	$V_{DD} \times 0.7$		V_{DD}	V
Low level input voltage	V_{iL}	0		$V_{DD} \times 0.3$	V
Clock frequency	f	0.1	12	25	MHz
Sensor integration time	t_{int}		0.3		ms
Wavelength of light source	λ	400		700	nm
Clock pulse high duty cycle		25	50	75	%
Operating free-air temperature	T_A	0		50	°C

Table 4. Recommended operating conditions.

Timing Diagram (for chip)

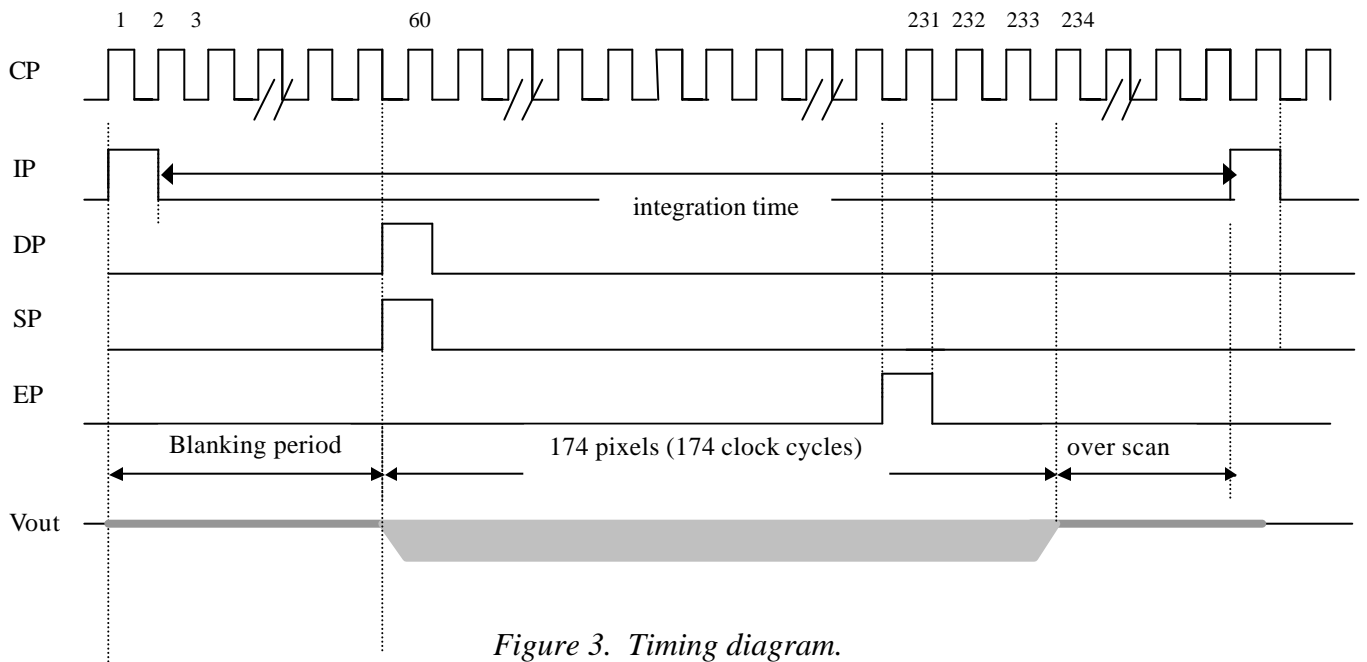


Figure 3. Timing diagram.

Switching Characteristics

Item	Description	Symbol	Min	Typ.	Max	Unit
1	Clock cycle time	t_o		0.5		μs
2	Clock pulse duty cycle: t_w / t_o			50		%
3	Clock pulse width	t_w		250		ns
4	ϕ_{Sp} setup time	t_{ss}	50			ns
5	ϕ_{Sp} hold time	t_{sh}	50			ns
6	Video digital delay time	t_{pd}		10		ns
8	Video signal stable time	t_{s}		15		ns

Table 5. Switching characteristics

Switching Waveforms

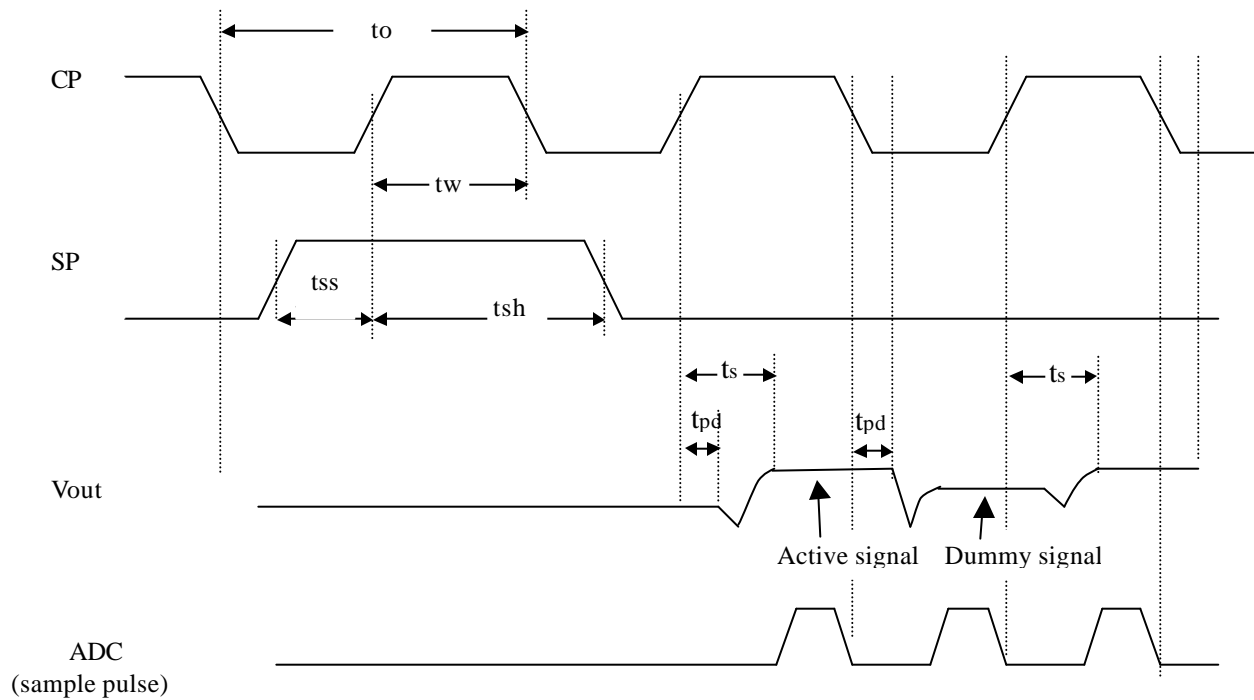


Figure 4. Switching waveforms

CIS Module Schematic

Figure 5 shows the schematic of the Contact Image Sensor (CIS) module using C212 sensor chip. On the first chip, pin 1 is connected to pin 2. On all other chips, pin 2 is floating. The pin 14 on the first chip is connected to the pin 1 of second chip.

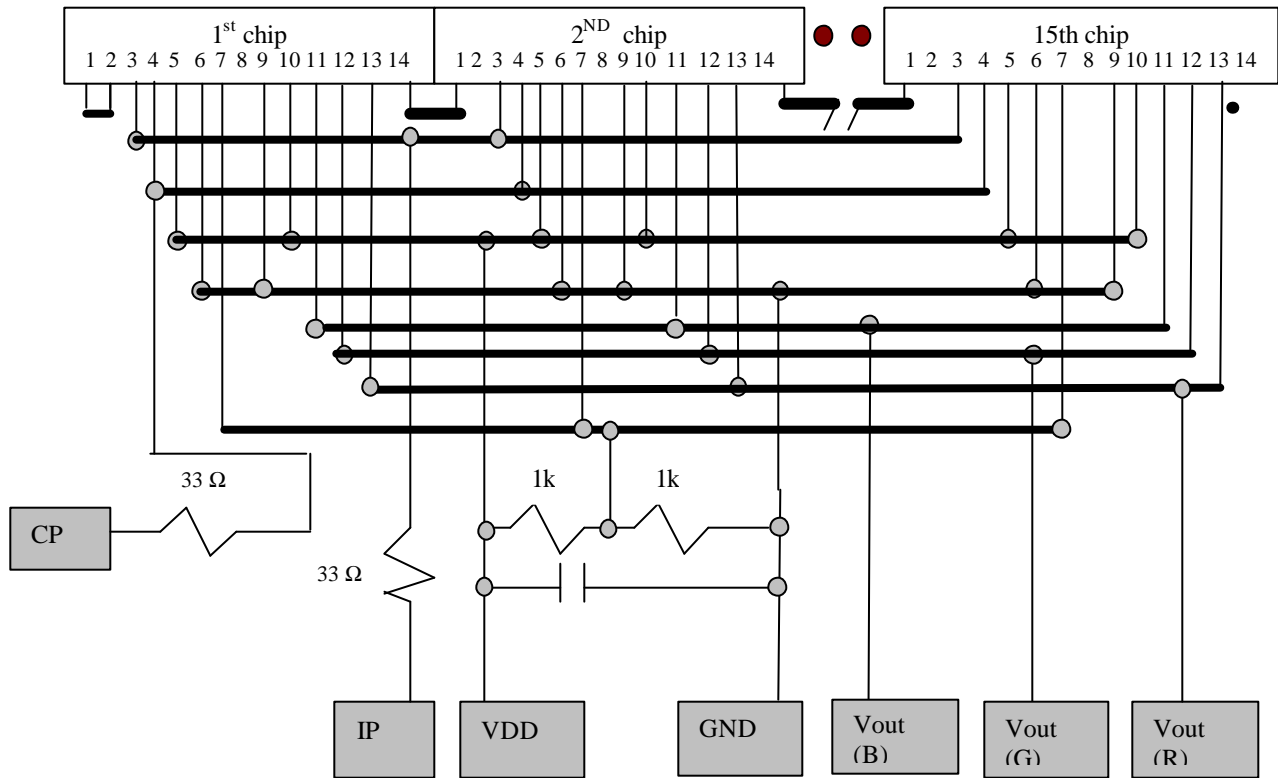
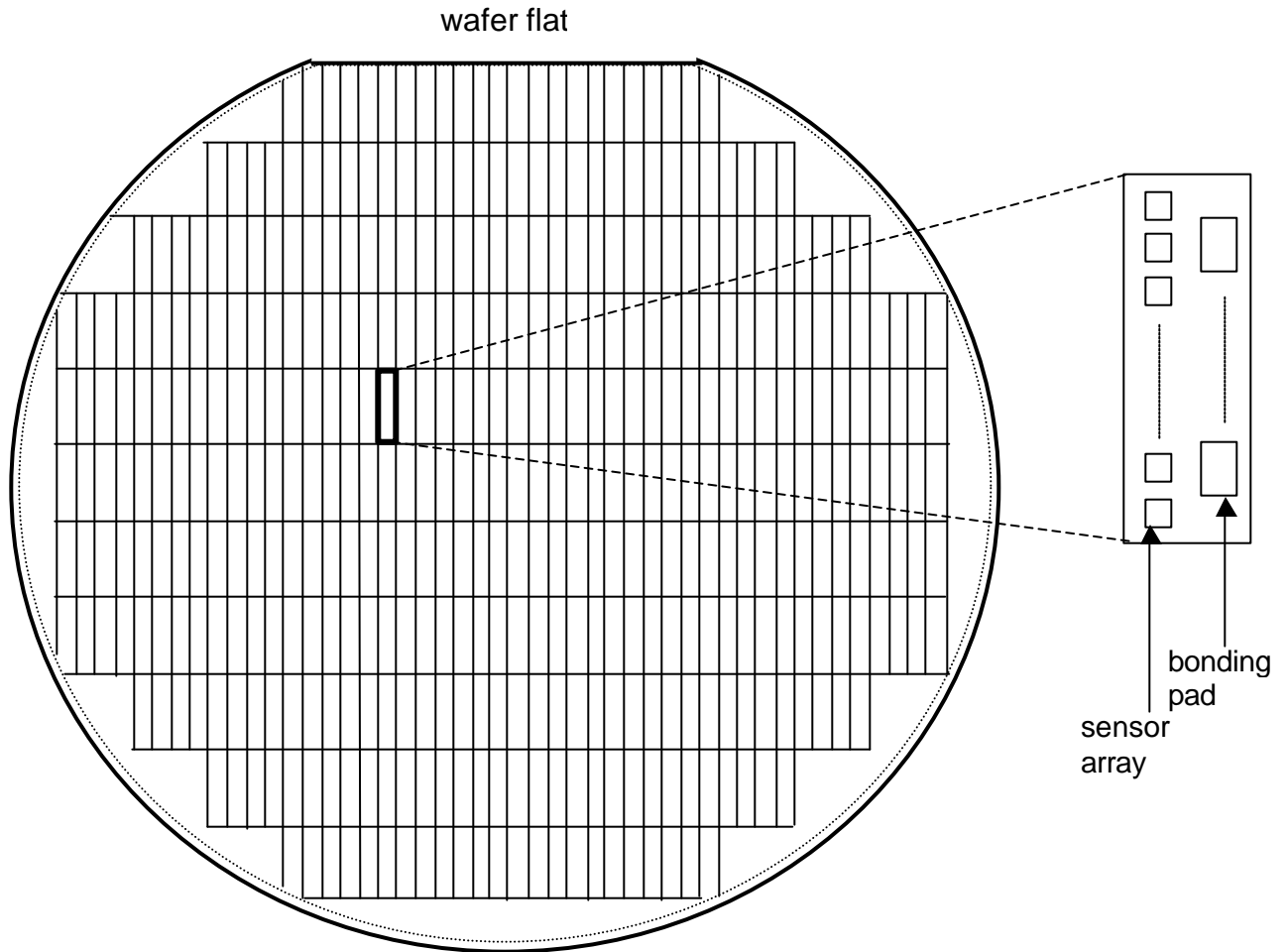


Figure 5. An example of the CIS module schematic.

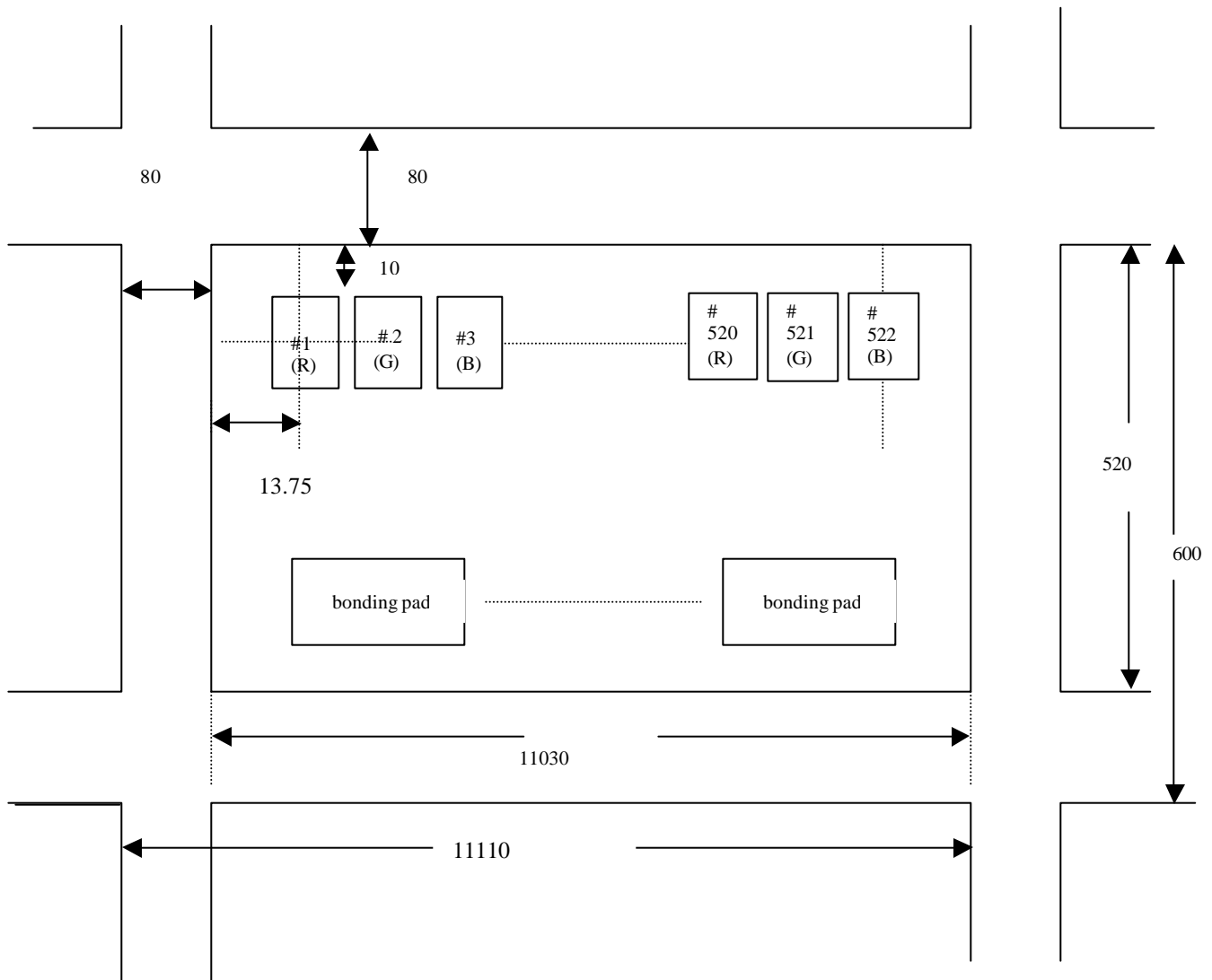
IC Chip Layout on a Wafer



Wafer thickness: 625 μm for color version
Wafer thickness: 350 μm for B/W version

Figure 6. Wafer map of C212 chip.

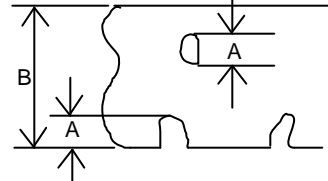
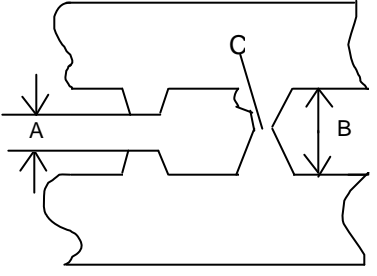

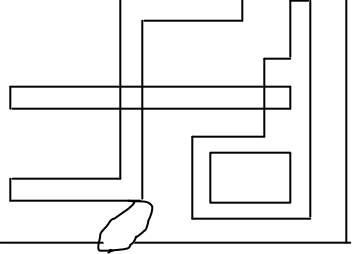
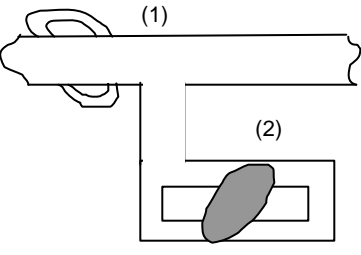
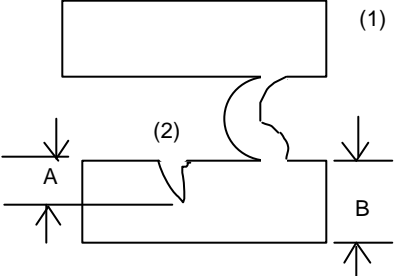
Scribe Line Layout Diagram (unit: micron)

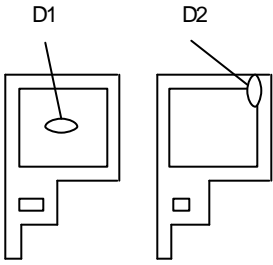
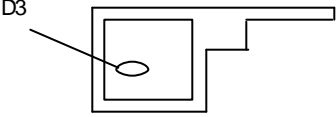
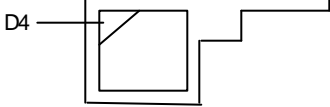
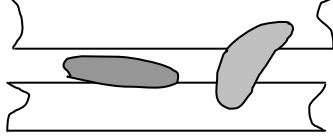
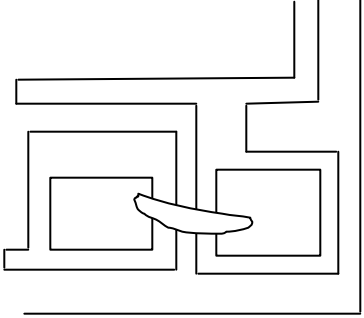
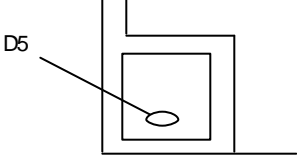


Sensor dimension: 20 μm x 42 μm

Figure 7. Scribe line layout diagram.

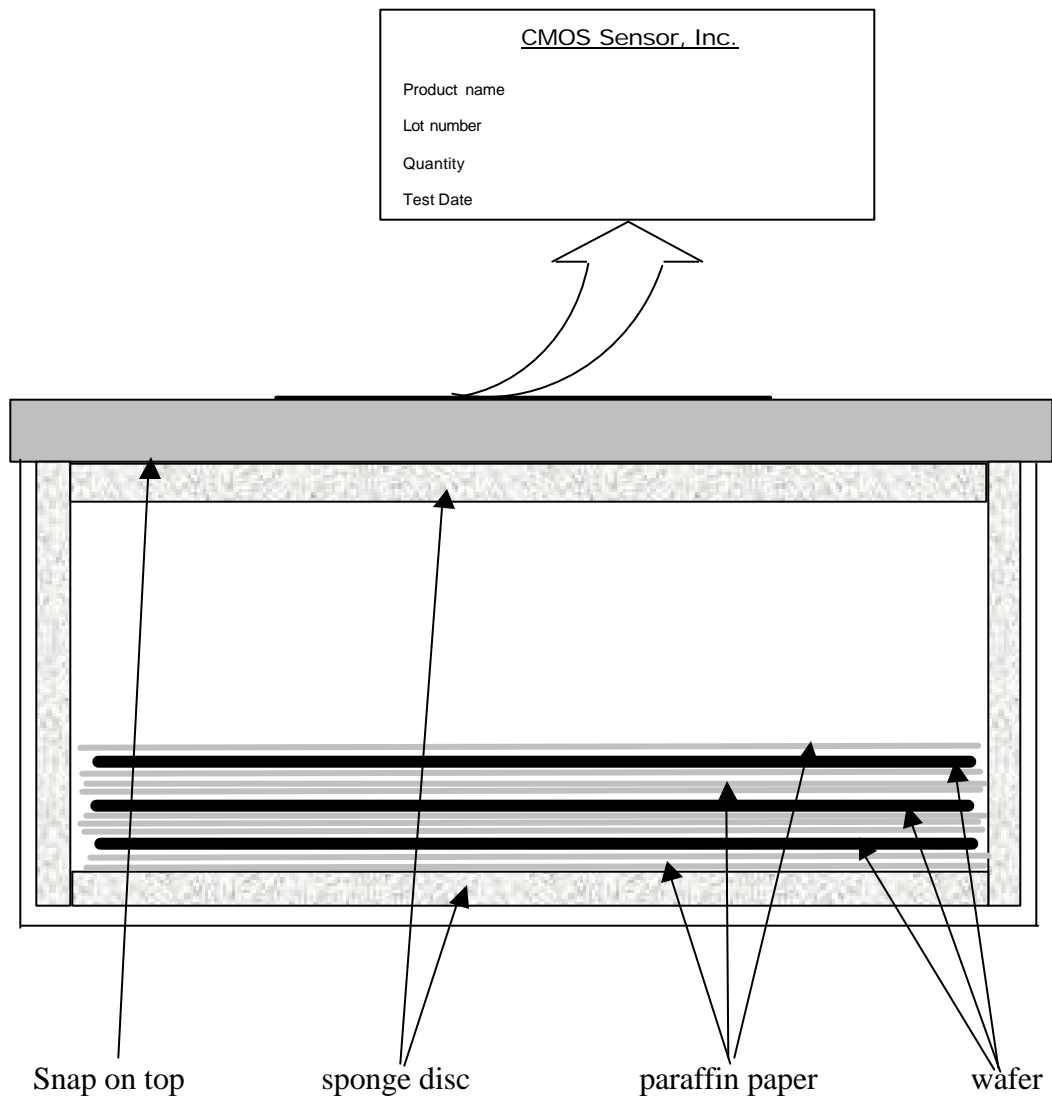
Microscope Inspection Specifications

No.	ITEMS	INSPECTION CRITERION	SIMPLIFIED DIAGRAM
1	BAD METAL LINE	(1) DEFICIENT AND VOID METAL LINE $A \geq B/2$	
		(2) PROXIMITY AND SHORTING OF METAL LINE $A \leq B/2$ C IS SHORTED	
		(3) HILLOCK	
		(4) METAL RESIDUES	
2	BAD OXIDE LAYER	(1) OXIDE LAYER VOID UNDER METAL LINE	
		(2) OXIDE LAYER VOID ON METAL LINE TO THE ACTIVE DEVICE	
3	BAD DIFFUSION	(1) SHORT BETWEEN TWO DIFFUSION REIGONS	
		(2) DEFICIT DIFFUSION REGION $A \geq B/2$	

No.	ITEMS	INSPECTION CRITERION	SIMPLIFIED DIAGRAM
4	BAD BONDING PAD	(1) METAL LAYER VOID EITHER WITHIN PAD OR AT CORNER $D1 \geq D/5$ $D2 \geq D/5$ WHERE D IS THE SIZE OF THE BONDING PAD	
		(2) DISCOLORIZATION OF THE BONDING PAD METAL $D3 \geq D/5$	
		(3) MISSING BONDING PAD METAL	
5	BAD PASSIVATION LAYER	(1) PASSIVATION RESIDUE WITHIN PAD $D4 \geq D/5$ WHERE D IS THE PAD SIZE	
		(2) PASSIVATION VOID ON METAL LINES OR BE- TWEEN METAL LINES	
6	CONTAMINATION AND FOREIGN PARTICLES	(1) CONTAMINATION OR FOREIGN PARTICLE (a) WHICH HAS A SIZE GREATER THAN 50 MICRONS (b) WHICH CONNECTS BETWEEN TWO EXPOSED METAL PATTERNS	
		(2) CONTAMINATION OR FOREIGN PARTICLE ON THE BONDING PAD $D5 \geq D/5$	

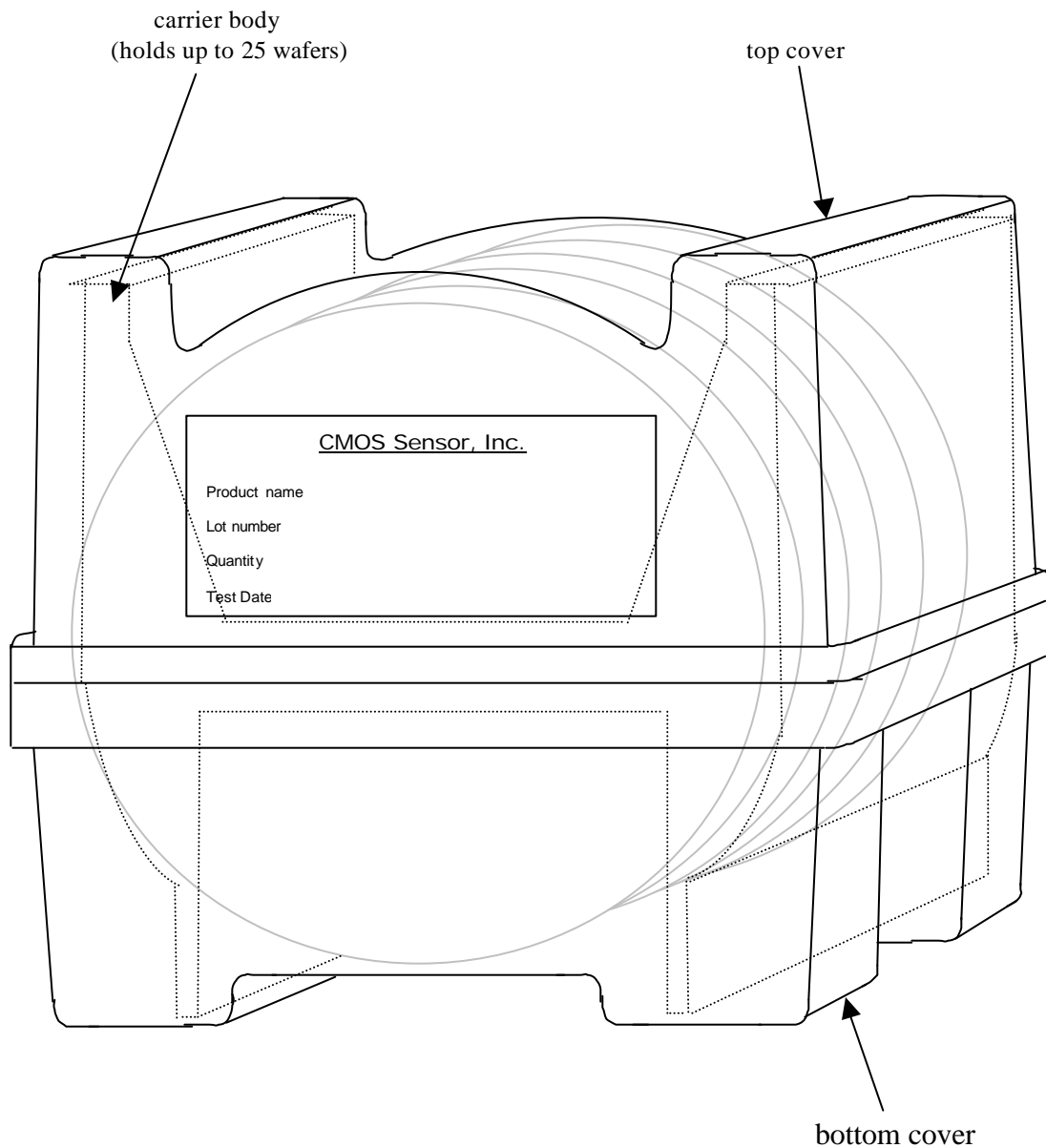
Shipping Package

1. Basically, wafers in the containers shown are manufactured under the same conditions at the same time.
2. Wafers may be shipped in either of two package types:
 - (1) a round shipping package.
 - (2) a molded wafer shipper.



(repeat paraffin paper and wafer layers up to 100 wafers)

(1) ROUND SHIPPING PACKAGE



(2) MOLDED WAFER SHIPPER

2. Identification

A label should be attached to each shipping container.
The label must include the following items:

- (1) product name
- (2) lot number
- (3) quantity
- (4) test date

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