

Preliminary

# Linear Image Sensor

Product Name

**C208 single chip**

Approval

Notes

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All specifications of this device are subject to change without notice.

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## Revision control sheet

| Rev | Date | From | Description |
|-----|------|------|-------------|
|     |      |      |             |

**C208 single chip**  
**PRODUCT SPECIFICATIONS**

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## Introduction

### 1. Features:

- 192 x 1 image sensing elements
- 600 dots per inch (dpi) resolution
- 42.15  $\mu\text{m}$  pixel center-to-center spacing
- High dynamic range > 1000
- On-chip timing and clock driver
- Active pixel readout
- Good linearity
- Single 5 V power supply
- Low power consumption: 10mW maximum
- Differential analog output

### 2. Description:

C208 linear image sensor consists of buffer circuitry, timing generator, and active element array. The timing generator provides all the timing circuitry. The active element array consists of 192 active pixel sensors (APS), correlated doubled sampling (CDS) circuitry, buffer circuitry and an active element selector (AES). The CDS circuitry is made by S/H1 and S/H2 for reset noise cancellation. The center to center spacing between adjacent pixels is 42.15  $\mu\text{m}$ . The photodiodes are parallel-dump and serial-readout devices controlled by a series of active shift registers. The device is easy to operate. In addition to the 5V power supply, only 2 clock signals (input pulse  $\phi_{IP}$  and clock pulse  $\phi_{CP}$ ) are required to operate this device.

The device is designed for the application of silicon butting contact image sensors. The length of the chip is about 8 mm. One chip can be butted to another chip to form a long image sensor module. The length of the module can be extended to A6, A4, B4, A3, ... up to A0 size. For silicon butting CIS application, the end pulse ( $\phi_{EP}$ ) of the first chip is connected to the start pulse ( $\phi_{SP}$ ) of the next chip. This device can be used in a wide variety of applications such as color scanner, digital copier, mark reader, bar code reader, OCR, edge detector, positioning and optical encoding, etc.

## Functional Block Diagram

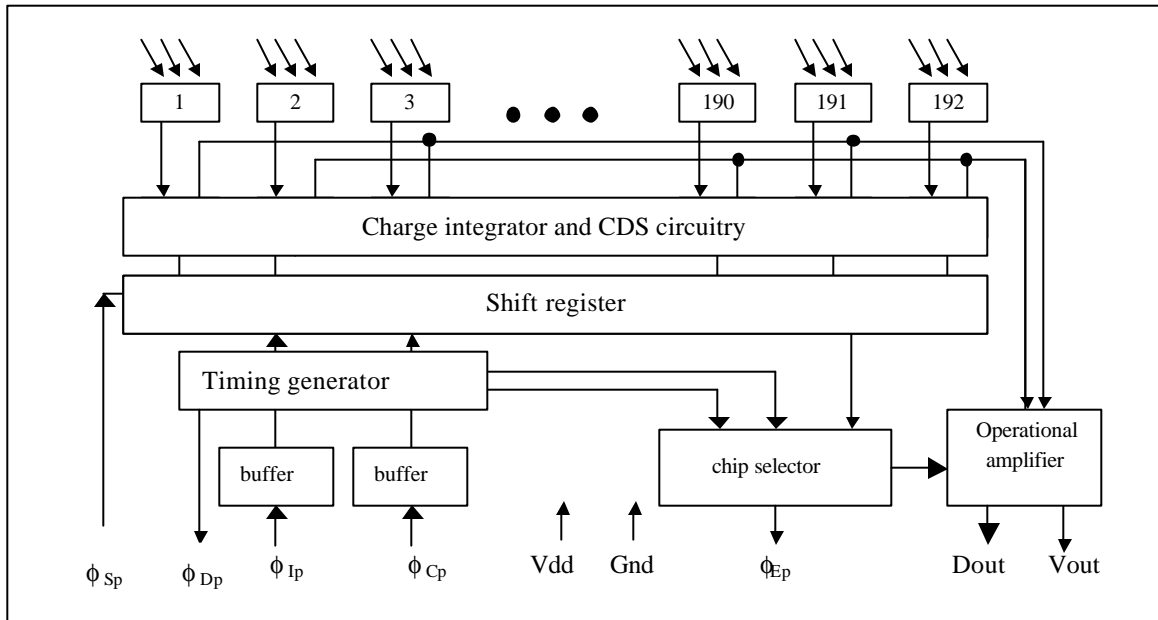


Figure 1. Functional Block Diagram

## Single chip Package Layout Diagram

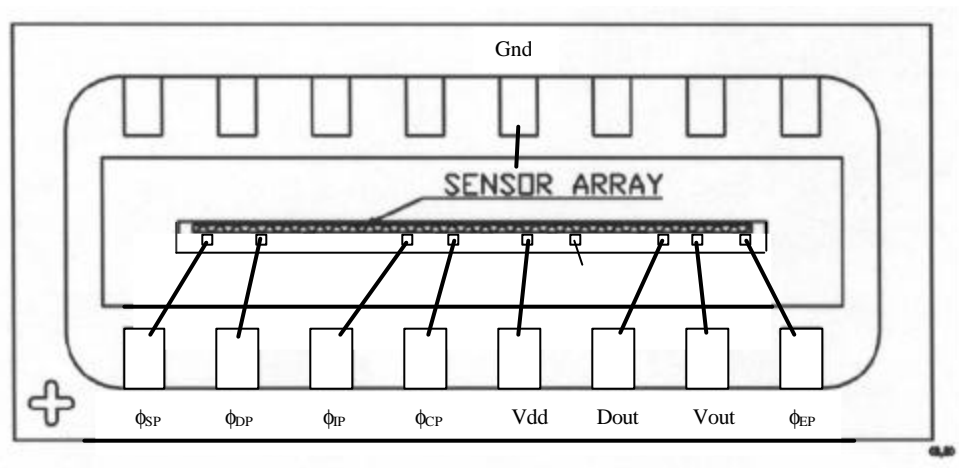


Figure 2. Single chip package layout diagram

## Terminal Description

| Terminal Number | Symbol      | Name                           | Description                              |
|-----------------|-------------|--------------------------------|--|
| 1               | $\phi_{Sp}$ | Start pulse terminal           | To apply a pulse to start signal readout |
| 2               | $\phi_{Dp}$ | Delay pulse output terminal    | Connect to pin # 1 for first chip        |
| 3               | $\phi_{Ip}$ | Input pulse terminal           | To apply a pulse to start integration    |
| 4               | $\phi_{Cp}$ | Clock pulse terminal           | To apply an external clock pulse to chip |
| 5               | Vdd         | Positive power supply terminal | To connect + 5 V normally                |
| 6               | Dout        | Dummy signal output terminal   | Send the dummy voltage signal out        |
| 7               | Vout        | Video signal output terminal   | Send the video voltage signal out        |
| 8               | $\phi_{Ep}$ | End of pulse terminal          | Send a pulse to indicate an end of scan  |
| 9 ~ 11          | NC          | No connection                  |  |
| 12              | Gnd         | Ground terminal                | To connect to 0 V normally               |
| 13 ~ 16         | NC          | No connection                  |  |

Table 1. Terminal Description

## Electro-Optical Characteristics

Test conditions:

Measured at  $\phi_{Cp} = 1000$  kHz, Vdd = 5V,  $t_{int}^{*(1)} = 2$  ms,  $\lambda^{*(2)} = 565$  nm,  $C_{ext}^{*(3)} = 47$  pF, Gain  $^{*(4)} = 2$ , TA  $^{*(5)} = 25$  °C, light intensity = 25 LUX.

[See readout circuitry (unless otherwise noted).]

| Symbol               | Description                              | Test Conditions                | Min | Typ | Max | Unit |
|----------------------|--|--------------------------------|-----|-----|-----|------|
| $V_c^{*(6)}$         | Compensated analog output voltage        | Light on                       | 400 | 500 | 600 | mV   |
| $U_c^{*(7)}$         | Compensated nonuniformity                | Pixel 2 ~ 191**, within a chip | -20 | --- | +20 | %    |
| $U_{p\_5pix}^{*(8)}$ | 5 pixel white level nonuniformity        | Every 5 pixels, within a chip  | -10 | --- | 10  | %    |
| $U_{cadj}^{*(9)}$    | Compensated adjacent pixel nonuniformity | Within a chip                  | -15 | --- | 15  | %    |
| $C_c^{*(10)}$        | Chip-chip compensated nonuniformity      | Within a wafer                 | -20 | --- | +20 | %    |
| $V_d^{*(11)}$        | Analog output voltage at dark level      | Light off                      | 35  | 40  | 45  | mV   |
| $U_d^{*(12)}$        | Dark signal nonuniformity                | Within a chip                  | --- | --- | 20  | mV   |
| $C_d^{*(13)}$        | Chip-chip dark signal nonuniformity      | Within a wafer                 | --- | --- | 10  | mV   |
| $I_{dd}$             | Power supply current                     |                                | --- | --- | 2   | mA   |

Table 2. Electro-Optical characteristics

Definition:

1.  $t_{int}$  is the integration time. It is equal to the interval between two start pulses.
2.  $\lambda$  is the wavelength of the light source.
3.  $C_{ext}$  is the off-chip load capacitance for  $I_{out}$ .
4. Gain is the gain of an off-chip video operation amplifier.
5. TA is the ambient temperature.
6.  $V_c = (V_{cmax} + V_{cmin}) / 2$   
where  $V_{cmax}$  is the maximum compensated voltage of the whole array.  
 $V_{cmin}$  is the minimum compensated voltage of the whole array.
7.  $U_c$  is the pixel-to-pixel compensated photo response nonuniformity within a chip.  
 $U_c = [((V_{cmax} - V_{cmin})/2) / V_c] \times 100\%$
8.  $U_{p\_5pix} = \text{Max} \{ \text{Max}[(V_p(i), V_p(i+1), \dots, V_p(i+4))] - \text{Min}[(V_p(i), V_p(i+1), \dots, V_p(i+4))] \} /$   
 $\{ \text{Max}[V_p(i), V_p(i+1), \dots, V_p(i+4)] + \text{Min}[V_p(i), V_p(i+1), \dots, V_p(i+4)] \}$   
( $i = 1, 2, \dots, 60$ )  
where  $V_p(i)$  is the video signal output of a pixel #  $i$   
 $V_p(i+1)$  is the video signal output of a pixel #  $(i+1)$   
 $\vdots$   
 $\vdots$   
 $V_p(i+4)$  is the video signal output of a pixel #  $(i+4)$
9.  $U_{cadj} = \text{Max} [ |(V_c(i) - V_c(i+1)) / V_c(i)| \times 100\%, (i = 2, 3, \dots, 63)$   
where  $V_c(i)$  is the compensated video signal output of a pixel #  $i$   
 $V_c(i+1)$  is the compensated video signal output of a pixel #  $(i+1)$
10.  $C_c$  is the chip-to-chip compensated photo response nonuniformity within a wafer  
 $C_c = [(V_c - V_{cavg}) / V_{cavg}] \times 100\%$   
where  $V_{cavg}$  is the average compensated output signal of all chips within a wafer
11.  $V_d = (V_{dmax} + V_{dmin}) / 2$   
where  $V_{dmax}$  is the maximum dark voltage of the whole array.  
 $V_{dmin}$  is the minimum dark voltage of the whole array.
12.  $U_d = V_{dmax} - V_{dmin}$
13.  $C_d$  is the chip-to-chip dark voltage nonuniformity within a wafer.  
 $C_d = V_d - V_{davg}$   
where  $V_{davg}$  is the average dark voltage of all chips within a wafer.

\*\* Pixel # 1 and # 192 measured by  $U_{p\_5pix}$

## Absolute maximum ratings:

|   |                |
|---|----------------|
| Power supply voltage, $V_{DD}$              | 7 V            |
| Power supply current, $I_{DD}$              | 60 mA          |
| Digital input voltage range, $V_{ih}$       | $V_{DD}$       |
| Digital input current range, $I_{ih}$       | 20 mA to 20 mA |
| Operating free-air temperature range, $T_A$ | 0 °C ~ 50 °C   |
| Storage temperature range, $T_{stg}$        | 25 °C ~ 70 °C  |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended operating conditions:

| Item                           | Symbol    | Min.                | Typ. | Max.                | Unit |
|--------------------------------|-----------|---------------------|------|---------------------|------|
| Power supply voltage           | $V_{DD}$  | 4.5                 | 5    | 5.5                 | V    |
| Power supply current           | $I_{DD}$  |                     |      |                     |      |
| Input voltage                  | $V_i$     |                     |      | $V_{DD}$            | V    |
| High level input voltage       | $V_{ih}$  | $V_{DD} \times 0.7$ |      | $V_{DD}$            | V    |
| Low level input voltage        | $V_{iL}$  | 0                   |      | $V_{DD} \times 0.3$ | V    |
| Clock frequency                | f         | 0.1                 |      | 5                   | MHz  |
| Sensor integration time        | $t_{int}$ |                     | 1.5  |                     | ms   |
| Wavelength of light source     | $\lambda$ | 400                 |      | 700                 | nm   |
| Clock pulse high duty cycle    |           | 25                  | 50   | 75                  | %    |
| Operating free-air temperature | $T_A$     | 0                   |      | 50                  | °C   |

Table 3. Recommended operating conditions.

## Timing Diagram

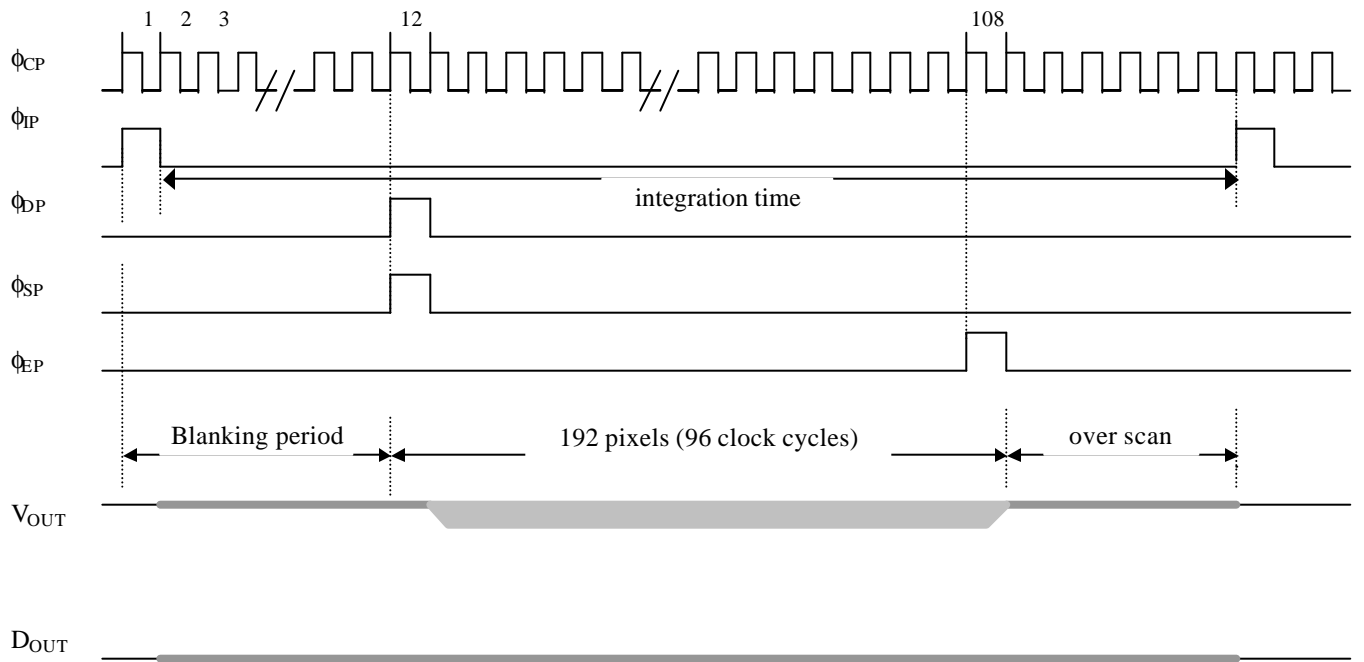


Figure 3. Timing Diagram

## Readout Circuitry

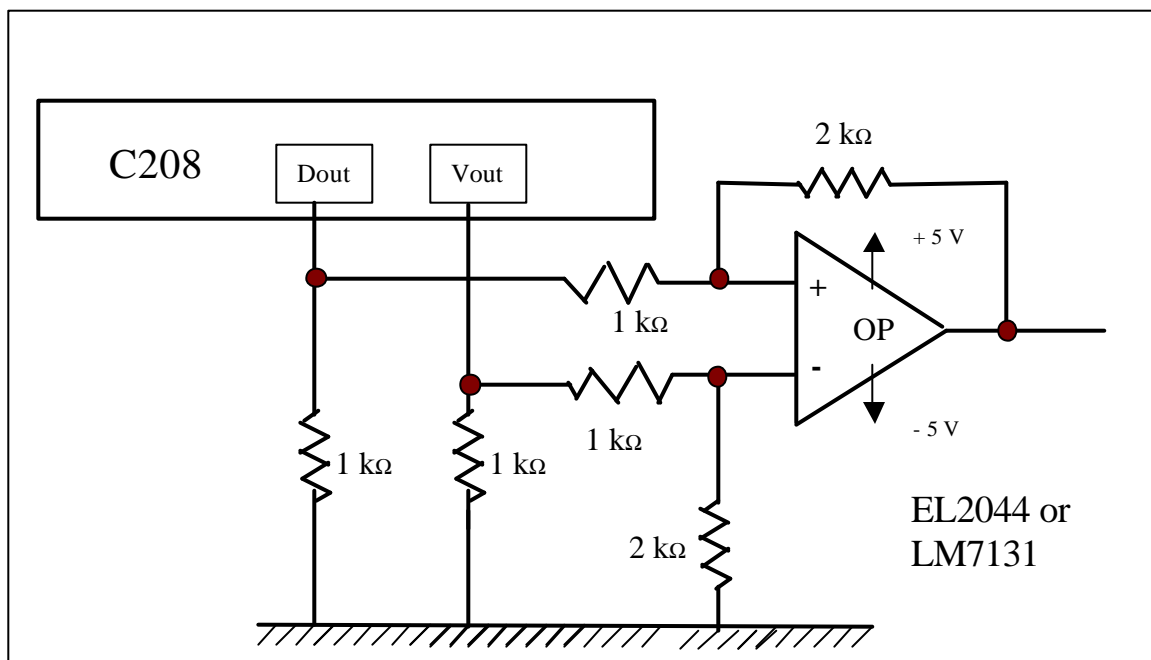


Figure 4. Readout Circuitry

## Switching Characteristics

| Item | Description                         | Symbol   | Min | Typ. | Max | Unit          |
|------|-------------------------------------|----------|-----|------|-----|---------------|
| 1    | Clock cycle time                    | $t_o$    |     | 1    |     | $\mu\text{s}$ |
| 2    | Clock pulse duty cycle: $t_w / t_o$ |          |     | 50   |     | %             |
| 3    | Clock pulse width                   | $t_w$    |     | 500  |     | ns            |
| 4    | $\phi_{Sp}$ setup time              | $t_{ss}$ | 50  |      |     | ns            |
| 5    | $\phi_{Sp}$ hold time               | $t_{sh}$ | 50  |      |     | ns            |
| 6    | Video digital delay time            | $t_d$    |     | 50   |     | ns            |
| 8    | Video signal stable time            | $t_s$    |     |      |     | ns            |

Table 4. Switching characteristics

## Switching Waveforms

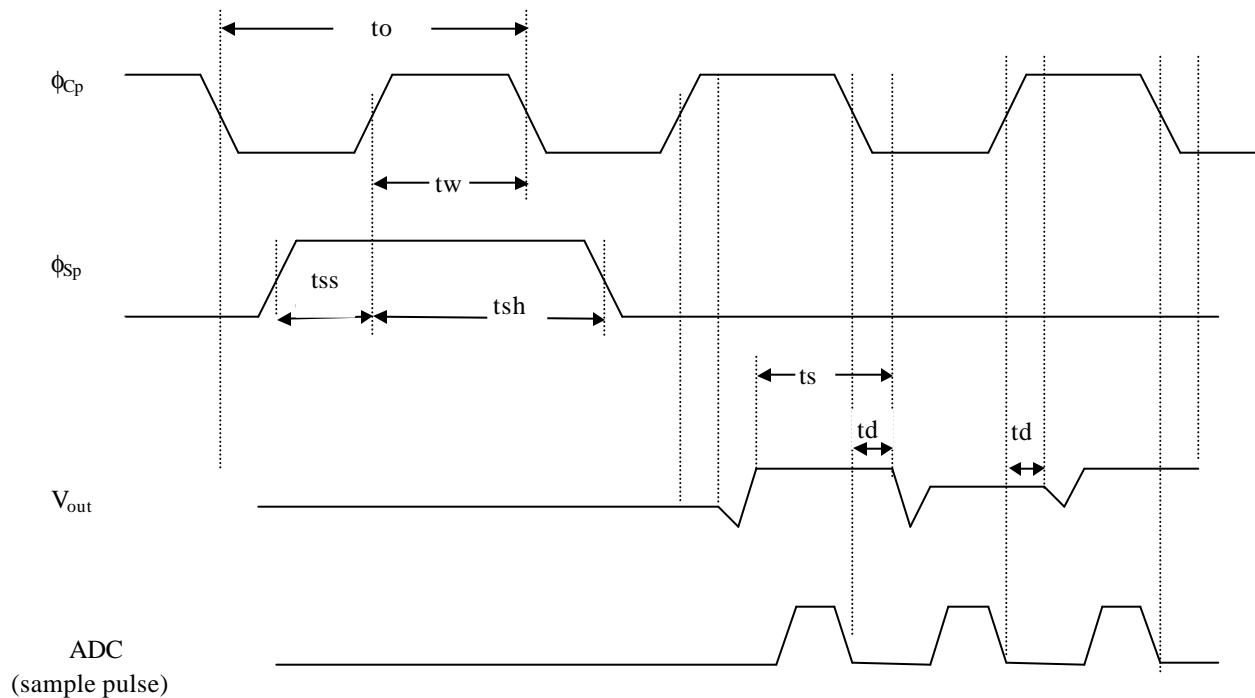


Figure 5. Switching waveforms

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