Preliminary

Linear Image Sensor

Product Name	**C208**

Approval	Notes

CMOS Sensor Inc.
20045 Stevens Creek Blvd.,
Suite 1A
Cupertino, CA., 95014
Tel: (408) 366-2898
Fax: (408) 366-2698

Approved	Checked	Designed

Issued	June, 2001	Revision No.	V1.0

All specifications of this device are subject to change without notice.

Revision control sheet

Revision No.	Date	Item of change and content	Reason	Approved	Designed

QUALITY DOCUMENT

This document applies to the image sensor products of CMOS Sensor Inc., regarding the product applications, product specifications and quality assurance to ensure customer satisfaction.

Quality Specifications

1. Reliability Test Items

No.	Test Item	Test Conditions	Test Time	LTFR
1	Biased high temp./ humidity	Ta = 85 °C, RH = 85%, Vabsmax x 0.9	1000 hr.	10%
2	Biased high temperature	Ta = 125 °C, Vabsmax x 0.9	1000 hr.	10%
3	Normal operation	Ta = 25 °C, Vopmax	1000 hr.	10%
4	EDS	C = 200 pF, V = 200 V to Vss, Vdd	1	
5	Latch-up	V = ± 100V, C = 200 pF, V = Vopmax	1	

Note: Vabsmax: Absolute maximum voltage.
Vopmax: Maximum operational voltage.
Test Conditions can be discussed between two parties.

2. Conditions:
   If there is any disagreement on any test item described above, both parties should discuss the issues to solve the discrepancies.

Outgoing Inspection

1. Every wafer of the same lot should be processed in the same lot during manufacturing.

2. Inspection Items
   2.1. Visual Inspection:
      1) Lot numbers, wafer numbers.
      2) Wafer surface color.
      3) Surface conditions:
         (a) Contamination
         (b) Particle
         (c) Scratch
   2.2. Microscope Inspection:
      1) Instrument: Metallurgical microscope.
      2) Magnitude: x100 in bright field.
      3) Criterion: See attached microscope inspection criterion.
      4) Inspection method: Five points inspection as shown in Figure 1:
         1: Center 2: Top 3: Bottom
         4: Left with more than 10 mm from the wafer edge.
         5. Right with more than 10 mm from the wafer edge

20045 Stevens Creek Blvd., Suite 1A, Cupertino, CA., 95014 USA Tel: (408) 366-2898; Fax: (408) 366-2698

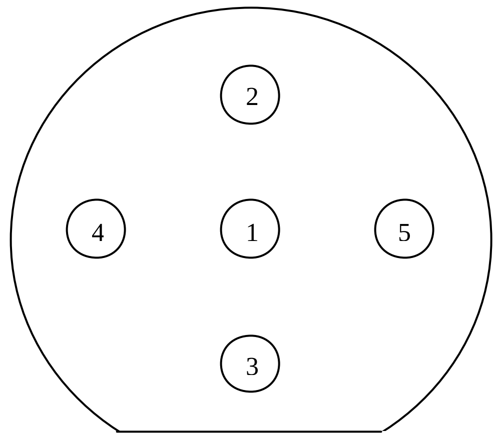


Figure 1. Five points inspection position on a wafer.

5) Sampling method:
   (a) 100% inspection for the lot with fewer than 5 wafers.
   (b) 5 wafers plus 20% of the lot size for the lot with more than 5 wafers.
6) Inspection pass criterion:
   (a) Per wafer: AQL = 0.4%
   (b) Per lot: AQL = 0.4%
7) Tools during wafer handling:
   (a) Tweezers or a vacuum van.
   (b) ESD gloves or finger cots

3. Wafer shipping criterion
   3.1. Per wafer: The yield per individual wafer must be greater than 60%.
   3.2. Per lot: The average lot yield must be greater than 60%.

4. Discrepancy resolution
   4.1. Any discrepancy should be investigated to determine the cause of this discrepancy and to explore the probable solutions to the issue.
   4.2. The return product will be analyzed to clarify the responsibility. If CMOS bears the responsibility, the deficit will be fully compensated.

5. Product Modification
   Any modification request from either party should be made in writing and may not be carried out without an agreement by both parties.

6. Product warranty
   Product is warranted for its performance according to the specs of this document for one year without any mishandling of the product during the warrant period after receiving the product.

7. Others
   This document can be modified if necessary when both parties agree.

C208
PRODUCT SPECIFICATIONS

20045 Stevens Creek Blvd., Suite 1A, Cupertino, CA., 95014 USA Tel: (408) 366-2898; Fax: (408) 366-2698

.

Introduction

1. Feature:
    - 192 x 1 image sensing elements
    - 600 dots per inch (dpi) resolution
    - 42.15 µm pixel center-to-center spacing
    - High dynamic range > 1000
    - On-chip timing and clock driver
    - Active pixel readout
    - Good linearity
    - Single 5 V power supply
    - Low power consumption: 10mW maximum
    - Differential analog output

2. Description:

C208 linear image sensor consists of buffer circuitry, timing generator, and active element array. The timing generator provides all the timing circuitry. The active element array consists of 192 active pixel sensors (APS), correlated doubled sampling (CDS) circuitry, buffer circuitry and an active element selector (AES). The CDS circuitry is made by S/H1 and S/H2 for reset noise cancellation. The center to center spacing between adjacent pixels is 42.15 µm. The photodiodes are parallel-dump and serial-readout devices controlled by a series of active shift registers. The device is easy to operate. In addition to the 5V power supply, only 2 clock signals (input pulse ϕ_{IP} and clock pulse ϕ_{CP}) are required to operate this device.

The device is designed for the application of silicon butting contact image sensors. The length of the chip is about 8 mm. One chip can be butted to another chip to form a long image sensor module. The length of the module can be extended to A6, A4, B4, A3, ... up to A0 size. For silicon butting CIS application, the end pulse (ϕ_{EP}) of the first chip is connected to the start pulse (ϕ_{SP}) of the next chip. This device can be used in a wide variety of applications such as color scanner, digital copier, mark reader, bar code reader, OCR, edge detector, positioning and optical encoding, etc.

Terminal Description

Terminal Number	Symbol	Name	Description
1	ϕ_{Sp}	Start pulse terminal	To apply a pulse to start signal readout
2	ϕ_{Dp}	Delay pulse output terminal	Connect to pin # 1 for first chip
3	ϕ_{Ip}	Input pulse terminal	To apply a pulse to start integration
4	ϕ_{Cp}	Clock pulse terminal	To apply an external clock pulse to chip
5	Vdd	Positive power supply terminal	To connect + 5 V normally
6	Gnd	Ground terminal	To connect to 0 V normally
7	Dout	Dummy signal output terminal	Send the dummy voltage signal out
8	Vout	Video signal output terminal	Send the video voltage signal out
9	ϕ_{Ep}	End of pulse terminal	Send a pulse to indicate an end of scan

Table 1. Terminal Description

Functional Block Diagram

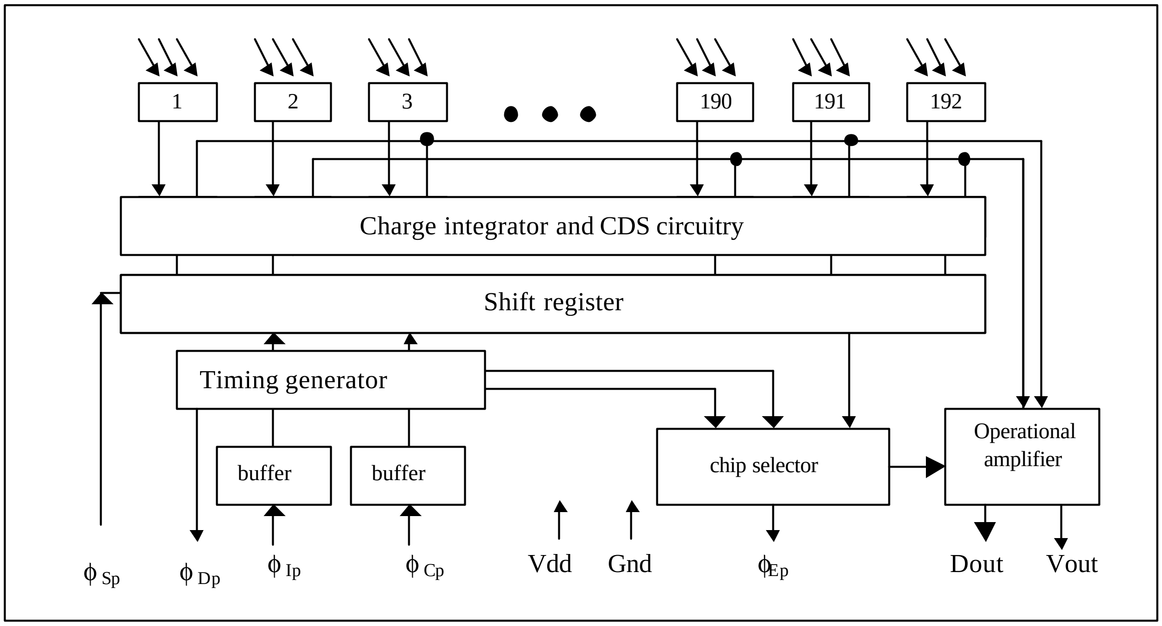


Figure 1. Functional Block Diagram

Bonding Pad Layout Diagram

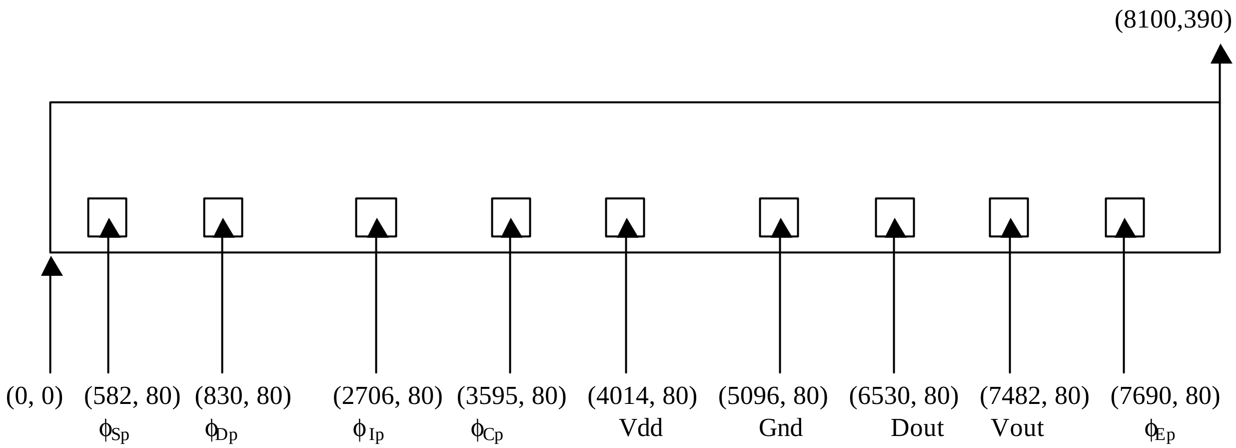


Figure 2. Bonding pad layout diagram

Bonding Pad Description

Pin #	Symbol	Location (x , y) in unit of mm	Description
1	ϕ_{Sp}	(582, 80)	Start pulse
2	ϕ_{Dp}	(830, 80)	Dummy output pulse
3	ϕ_{Ip}	(2706, 80)	Input pulse
4	ϕ_{Cp}	(3595, 80)	Clock pulse
5	Vdd	(4014, 80)	Power supply voltage: + 5V
6	Gnd	(5096, 80)	Ground : 0 V
7	Dout	(6530, 80)	Dummy signal output
8	Vout	(7482, 80)	Video signal output
9	ϕ_{Ep}	(7690, 80)	End of pulse

Table 2. Bonding pad description

Note:
- Origin: (0 µm, 0 µm) at the lower, left side of the chip.
- Location: (x µm, y µm) is measured at the center of the pad.
- Pad size: (125 µm by 90 µm)
- Chip size: (8100 µm by 390 µm) for the chip.
  (150 µm by 450 µm), including the scribe lines.

Electro-Optical Characteristics

Test conditions:
Measured at ϕ_{Cp} = 1000 kHz, Vdd = 5V, t_{int} *(1) = 2 ms, λ*(2) = 565 nm, C_{ext} *(3) = 47 pF, Gain*(4) = 2, TA*(5) = 25 °C, light intensity = 25 LUX.
[See readout circuitry (unless otherwise noted).]

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_c *(6)	Compensated analog output voltage	Light on	400	500	600	mV
U_c *(7)	Compensated nonuniformity	Pixel 2 ~ 191**, within a chip	-20	---	+20	%
U_{p_5pix} *(8)	5 pixel white level nonuniformity	Every 5 pixels, within a chip	-10	---	10	%
U_{cadj} *(9)	Compensated adjacent pixel nonuniformity	Within a chip	-15	---	15	%
C_c *(10)	Chip-chip compensated nonuniformity	Within a wafer	-20	---	+20	%
V_d *(11)	Analog output voltage at dark level	Light off	35	40	45	mV
U_d *(12)	Dark signal nonuniformity	Within a chip	---	---	20	mV
C_d *(13)	Chip-chip dark signal nonuniformity	Within a wafer	---	---	10	mV
I_{dd}	Power supply current		---	---	2	mA

Table 3. Electro-Optical characteristics

Definition:

1. t_{int} is the integration time. It is equal to the internal between two start pulses.
2. λ is the wavelength of the light source.
3. C_{ext} is the off-chip load capacitance for $I_{out.}$
4. Gain is the gain of an off-chip video operation amplifier.
5. TA is the ambient temperature.
6. Vc = (Vcmax + Vcmin) / 2
   where Vcmax is the maximum compensated voltage of the whole array.
   Vcmin is the minimum compensated voltage of the whole array.
7. Uc is the pixel-to-pixel compensated photo response nonuniformity within a chip.
   Uc = [((Vcmax - Vcmin)/2) / Vc] x 100%
8. U_{p_5pix} = Max {Max[(Vp(i), Vp(i+1), …, Vp(i+4)] – Min[(Vp(i), Vp(i+1), …, Vp(i+4)]} ⁄
   {Max[Vp(i), Vp(i+1),…,Vp(i+4)]+Min[(Vp(i), Vp(i+1),…,Vp(i+4)]}
   (i = 1, 2, …, 60)
   where Vp(i) is the video signal output of a pixel # i
   Vp(i+1) is the video signal output of a pixel # (i+1)
   :
   :
   Vp(i+4) is the video signal output of a pixel # (i+4)
9. Ucadj = Max [|(Vc(i) - Vc(i+1)| / Vc(i)] x 100%, (i = 2, 3, …, 63)
   where Vc(i) is the compensated video signal output of a pixel # i
   Vc(i+1) is the ompensated video signal output of a pixel # (i+1)
10. Cc is the chip-to-chip compensated photo response nonuniformity within a wafer
    Cc = [(Vc - Vcavg) / Vcavg] x 100%
    where Vcavg is the average compensated output signal of all chips within a wafer
11. Vd = (Vdmax + Vdmin) / 2
    where Vdmax is the maximum dark voltage of the whole array.
    Vdmin is the minimum dark voltage of the whole array.
12. Ud = Vdmax – Vdmin
13. Cd is the chip-to-chip dark voltage nonuniformity within a wafer.
    Cd = Vd - Vdavg
    where Vdavg is the average dark voltage of all chips within a wafer.

** Pixel # 1 and # 192 measured by $Up_{\_5pix}$

Absolute maximum ratings:

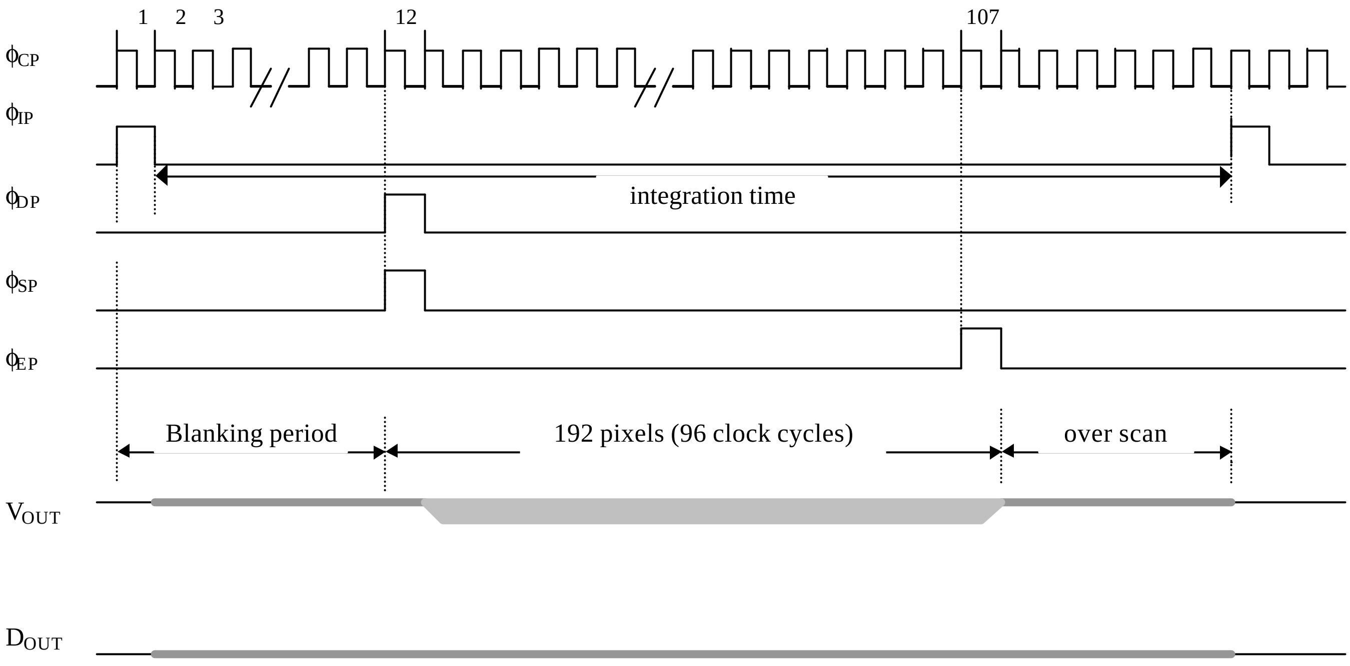
Power supply voltage, V_{DD} -- 7 V
Power supply current, I_{DD} --- 60 mA
Digital input voltage range, Vih -- V_{DD}
Digital input current range, Iih -- 20 mA to 20 mA
Operating free-air temperature range, TA --------------------------------- 0 °C ~ 50 °C
Storage temperature range, Tstg -- 25 °C ~ 70 °C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended operating conditions:

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.5	5	5.5	V
Power supply current	I_{DD}				
Input voltage	V_i			V_{DD}	V
High level input voltage	V_{ih}	V_{DD} x 0.7		V_{DD}	V
Low level input voltage	V_{iL}	0		V_{DD} x 0.3	V
Clock frequency	f	0.1		5	MHz
Sensor integration time	t_{int}		1.5		ms
Wavelength of light source	λ	400		700	nm
Clock pulse high duty cycle		25	50	75	%
Operating free-air temperature	TA	0		50	°C

Timing Diagram



Readout Circuitry

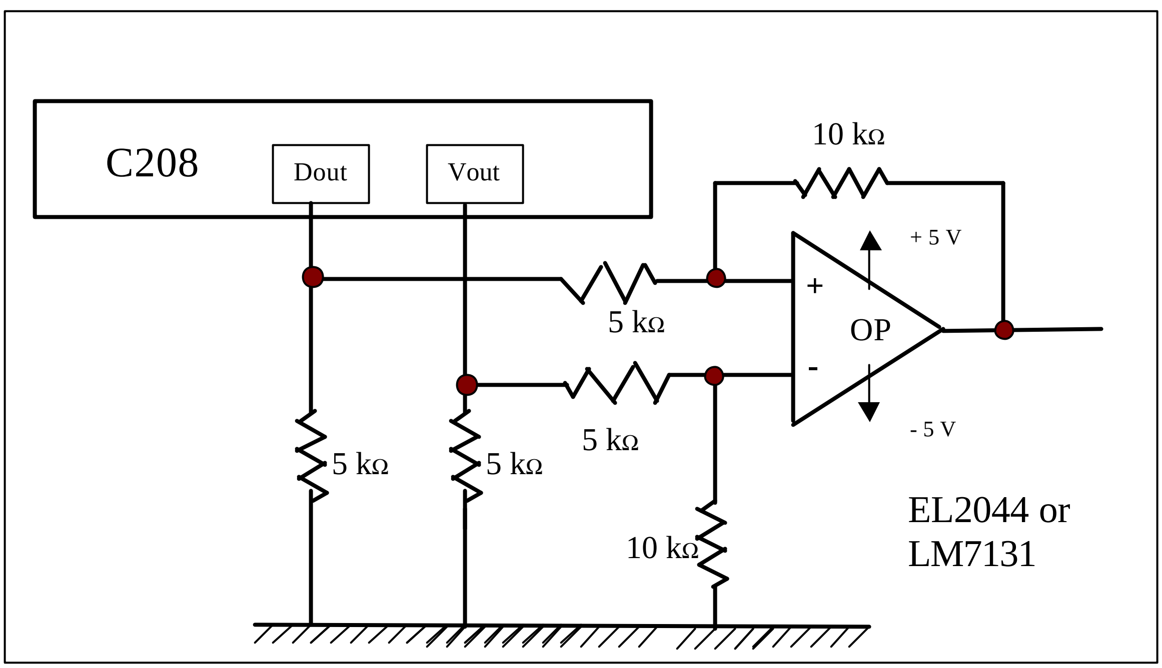


Figure 4. Readout circuitry

Switching Characteristics

Item	Description	Symbol	Min	Typ.	Max	Unit
1	Clock cycle time	to		1		µs
2	Clock pulse duty cycle: tw / to			50		%
3	Clock pulse width	tw		500		ns
4	ϕ_{Sp} setup time	tss	50			ns
5	ϕ_{Sp} hold time	tsh	50			ns
6	Video digital delay time	td		50		ns
8	Video signal stable time	ts				ns

Table 7. Switching characteristics

Switching Waveforms

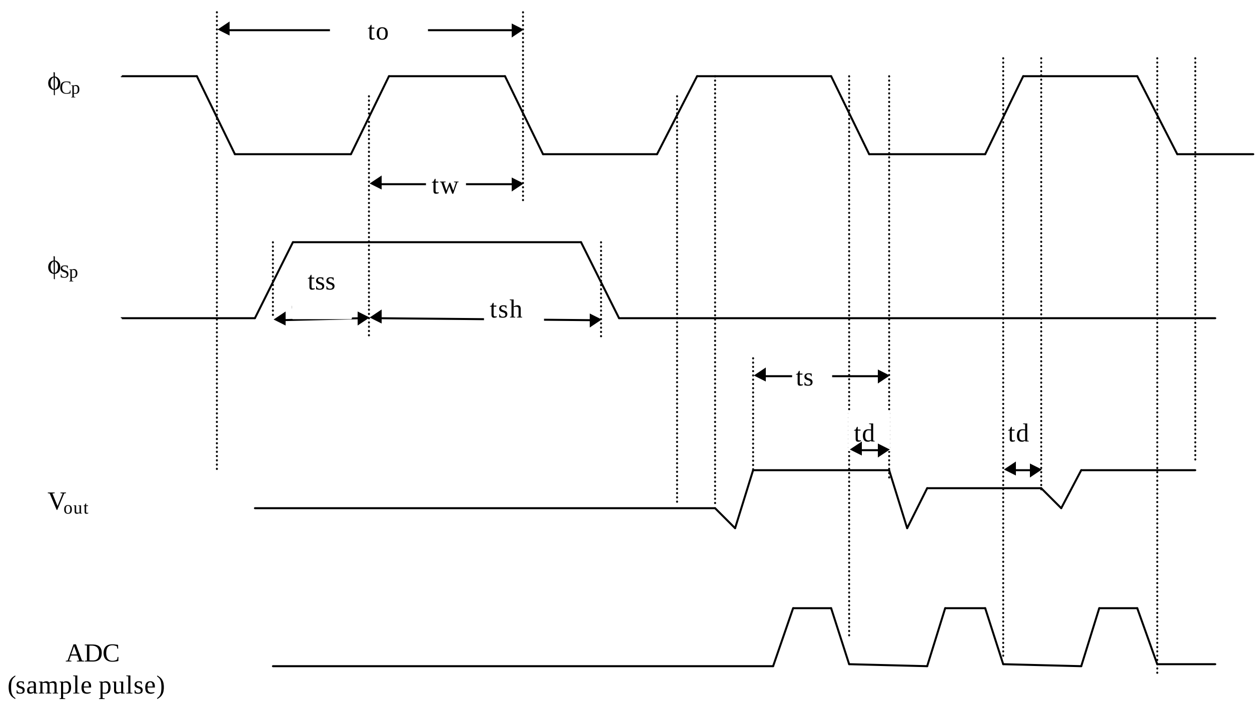


Figure 5. Switching waveforms

CIS Module Schematic

Figure 6 shows the schematic of the Contact Image Sensor (CIS) module using C208 sensor chip. On the first chip, pin 2 is connected to the pin 1. Except first chip, pin 2 is floating on other chip. The readout amplifier circuitry described in figure 4.

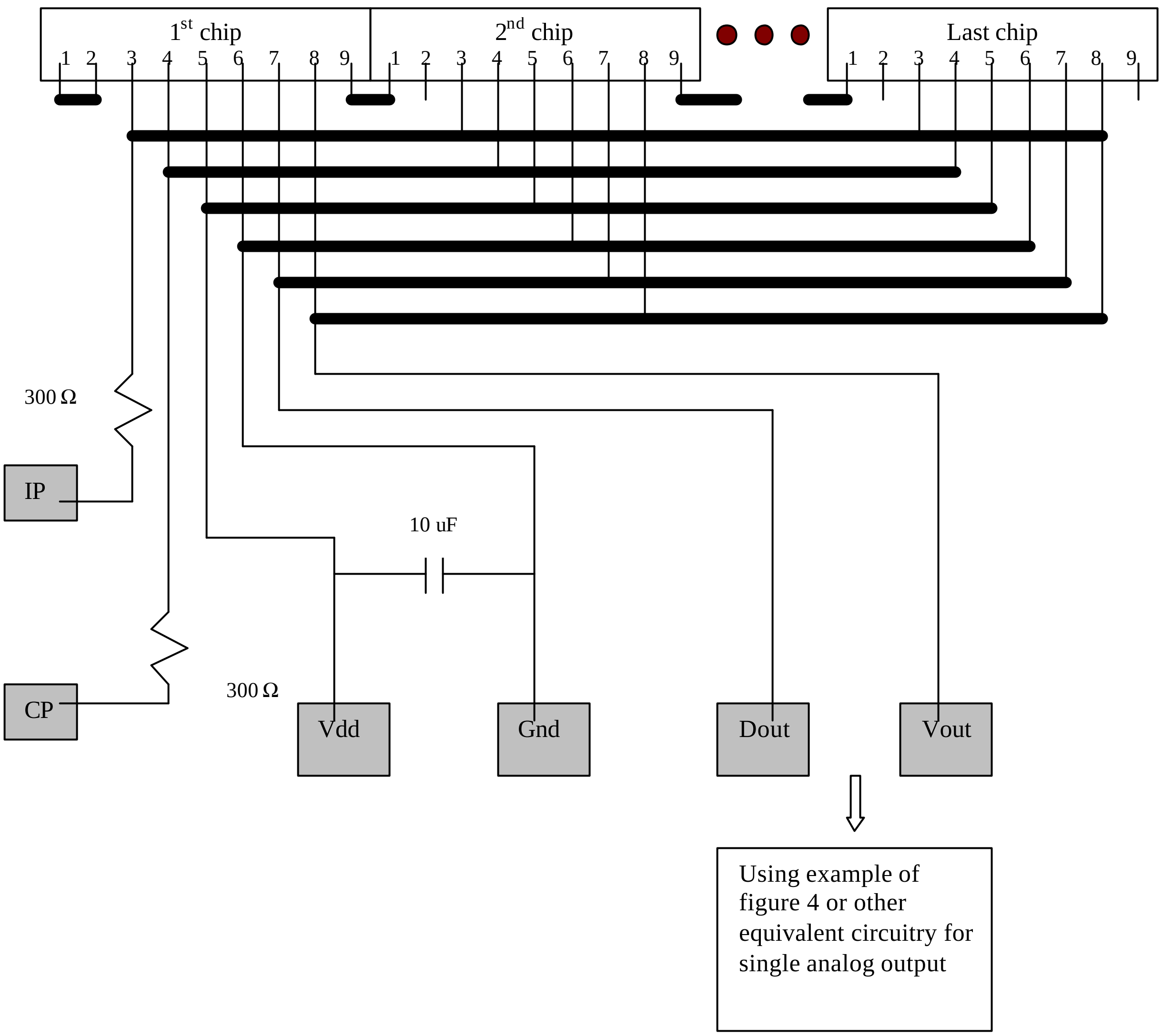
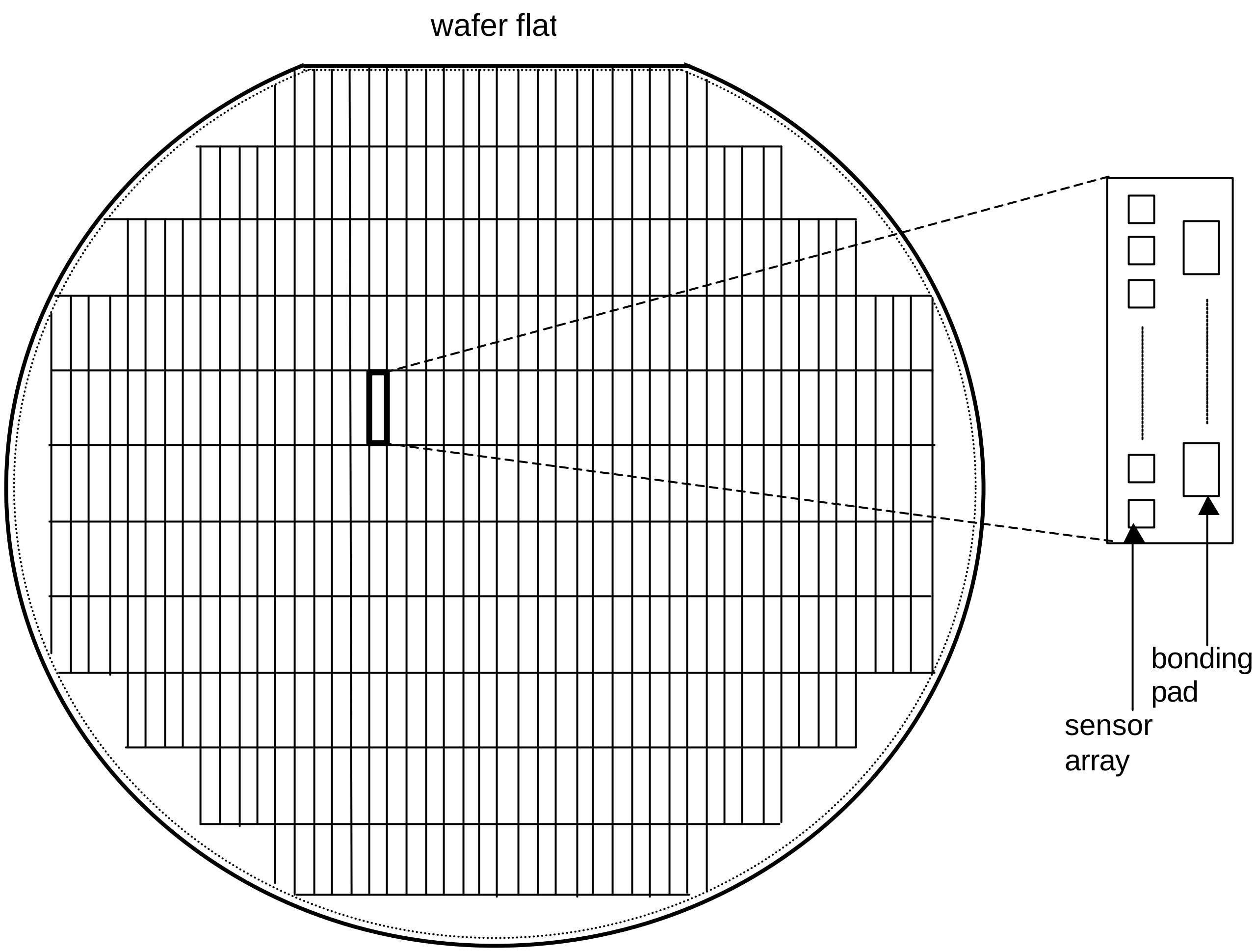


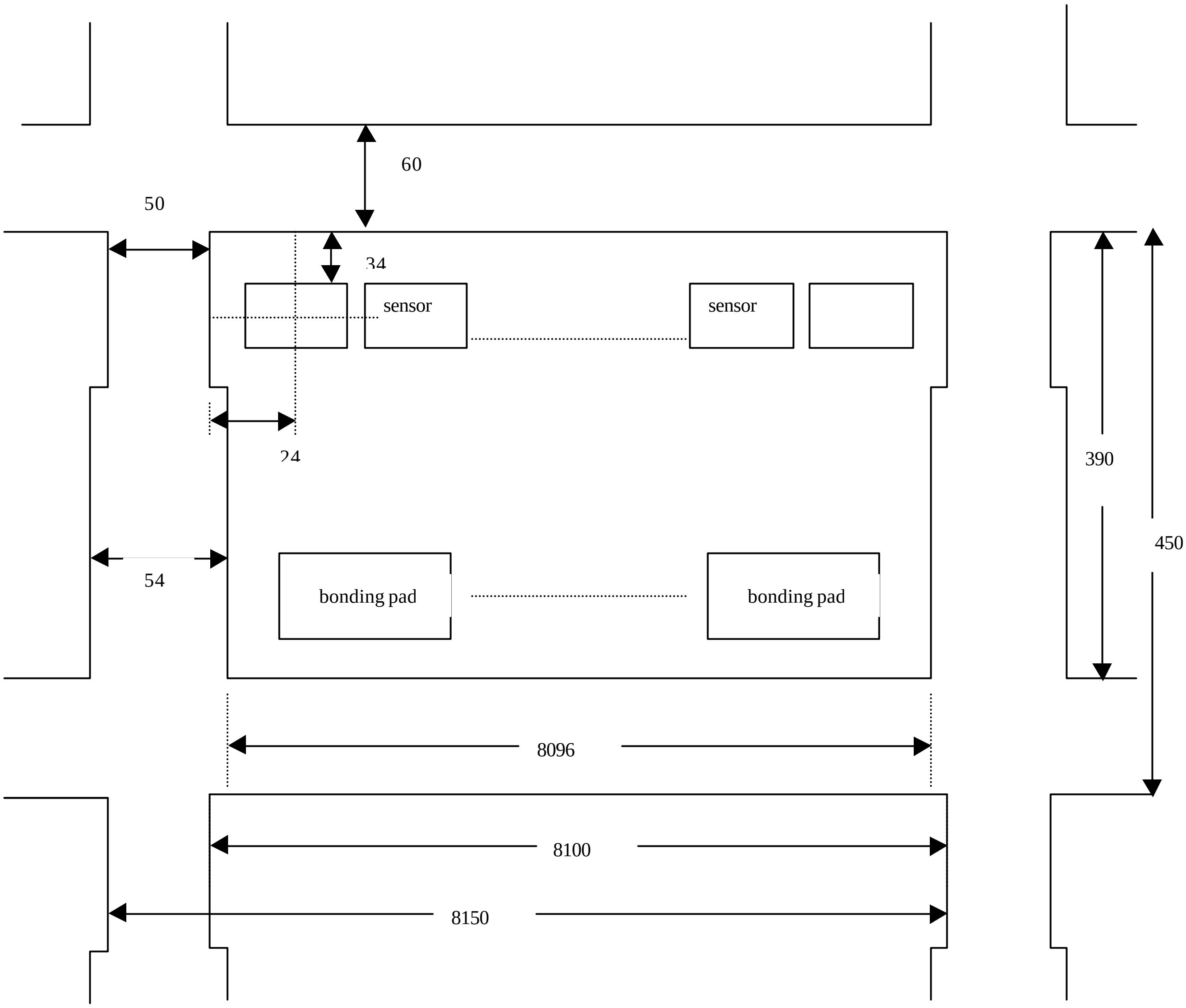
Figure 6. An example of the CIS module schematic.

IC Chip Layout on a Wafer



Wafer thickness: 350 µm

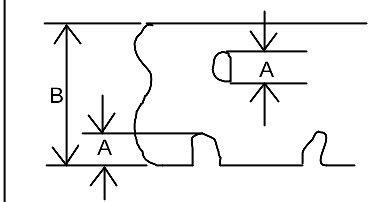
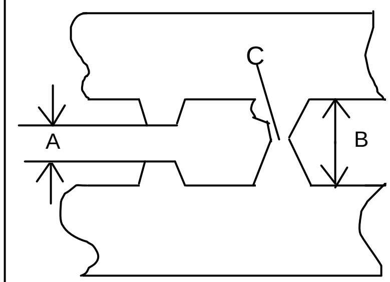
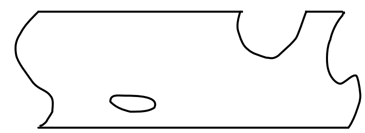
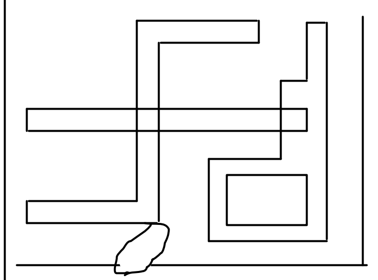
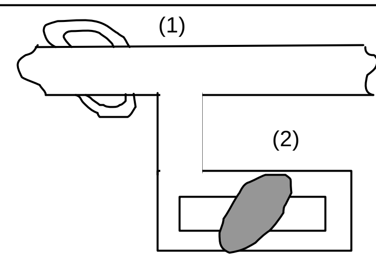
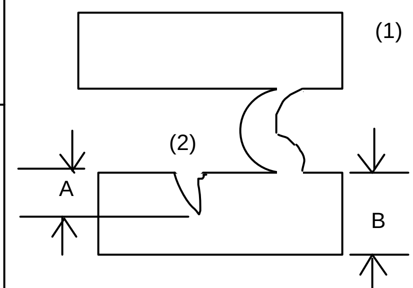
Scribe Line Layout Diagram (unit: micron)



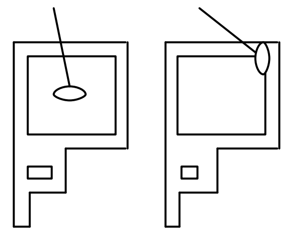
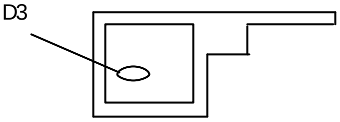
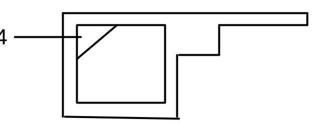
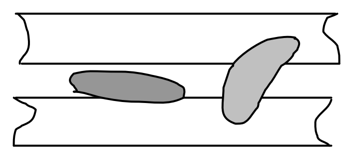
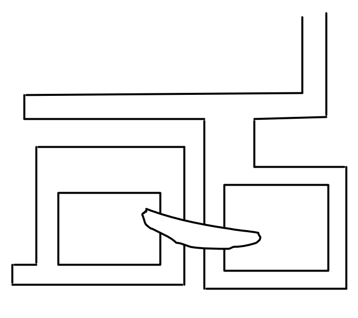
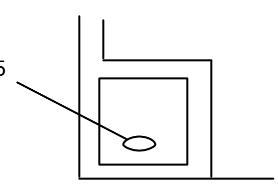
Sensor dimension: 36 µm x 38 µm

20045 Stevens Creek Blvd., Suite 1A, Cupertino, CA., 95014 USA Tel: (408) 366-2898; Fax: (408) 366-2698

Microscope Inspection Specifications

No.	ITEMS	INSPECTION CRITERION	SIMPLIFIED DIAGRAM
1	BAD METAL LINE	(1) DEFICIENT AND VOID METAL LINE A $\geq$ B/2	
		(2) PROXIMITY AND SHORTING OF METAL LINE A $\leq$ B/2 C IS SHORTED	
		(3) HILLOCK	
		(4) METAL RESIDUES	
2	BAD OXIDE LAYER	(1) OXIDE LAYER VOID UNDER METAL LINE	
		(2) OXIDE LAYER VOID ON METAL LINE TO THE ACTIVE DEVICE	
3	BAD DIFFUSION	(1) SHORT BETWEEN TWO DIFFUSION REIGONS	
		(2) DEFICIT DIFFUSION REGION A $\geq$ B/2	

20045 Stevens Creek Blvd., Suite 1A, Cupertino, CA., 95014 USA Tel: (408) 366-2898; Fax: (408) 366-2698

No.	ITEMS	INSPECTION CRITERION	SIMPLIFIED DIAGRAM
4	BAD BONDING PAD	(1) METAL LAYER VOID EITHER WITHIN PAD OR AT CORNER D1 $\geq$ D/5 D2 $\geq$ D/5 WHERE **D** IS THE SIZE OF THE BONDING PAD	
		(2) DISCOLORIZATION OF THE BONDING PAD METAL D3 $\geq$ D/5	
		(3) MISSING BONDING PAD METAL	
5	BAD PASSIVATION LAYER	(1) PASSIVATION RESIDUE WITHIN PAD D4 $\geq$ D/5 WHERE **D** IS THE PAD SIZE	
		(2) PASSIVATION VOID ON METAL LINES OR BE-TWEEN METAL LINES	
6	CONTAMINATION AND FOREIGN PARTICLES	(1) CONTAMINATION OR FOREIGN PARTICLE (a) WHICH HAS A SIZE GREATER THAN 50 MICRONS (b) WHICH CONNECTS BETWEEN TWO EXPOSED METAL PATTERNS	
		(2) CONTAMINATION OR FOREIGN PARTICLE ON THE BONDING PAD D5 $\geq$ D/5	

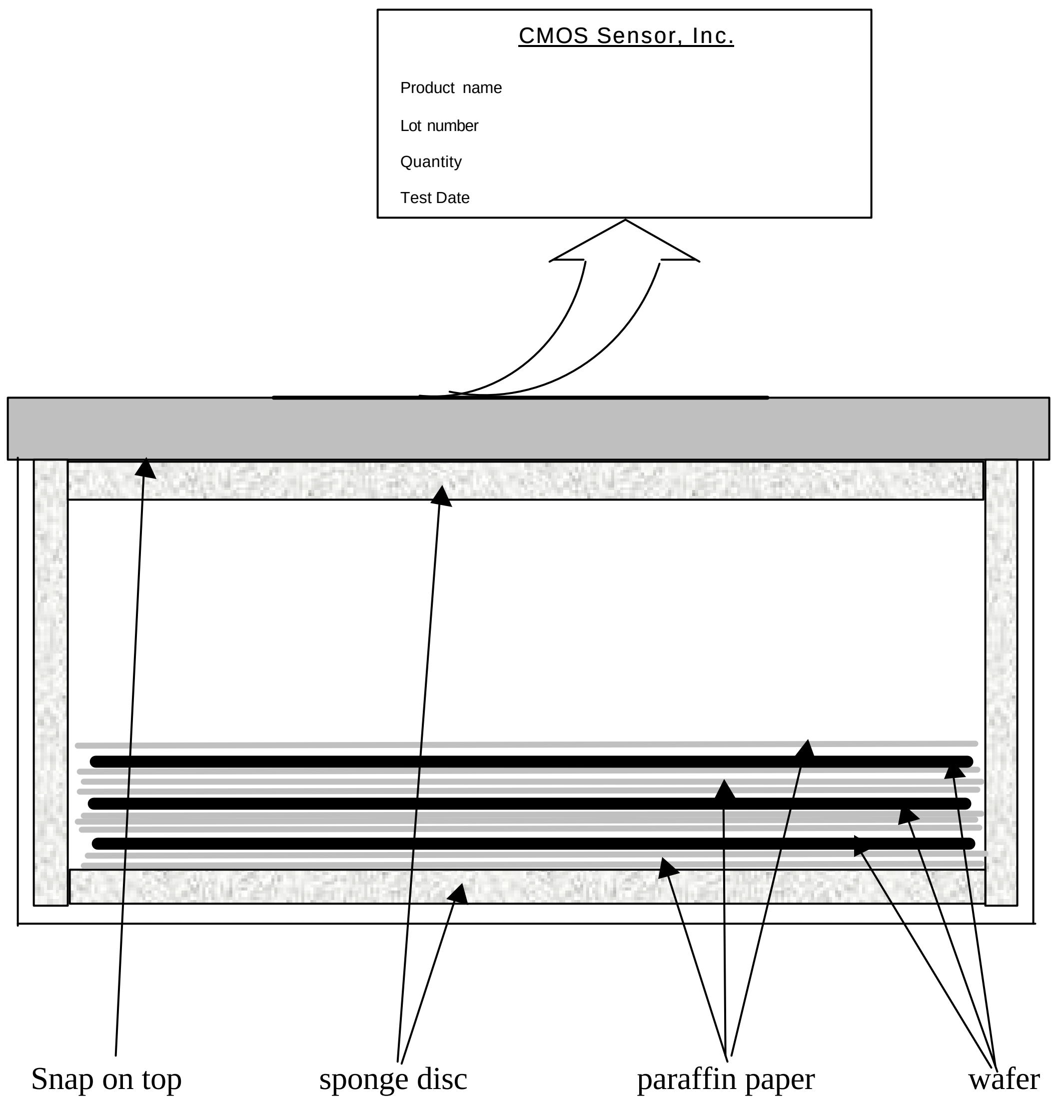
20045 Stevens Creek Blvd., Suite 1A, Cupertino, CA., 95014 USA Tel: (408) 366-2898; Fax: (408) 366-2698

Shipping Package

1. Basically, wafers in the containers shown are manufactured under the same conditions at the same time.

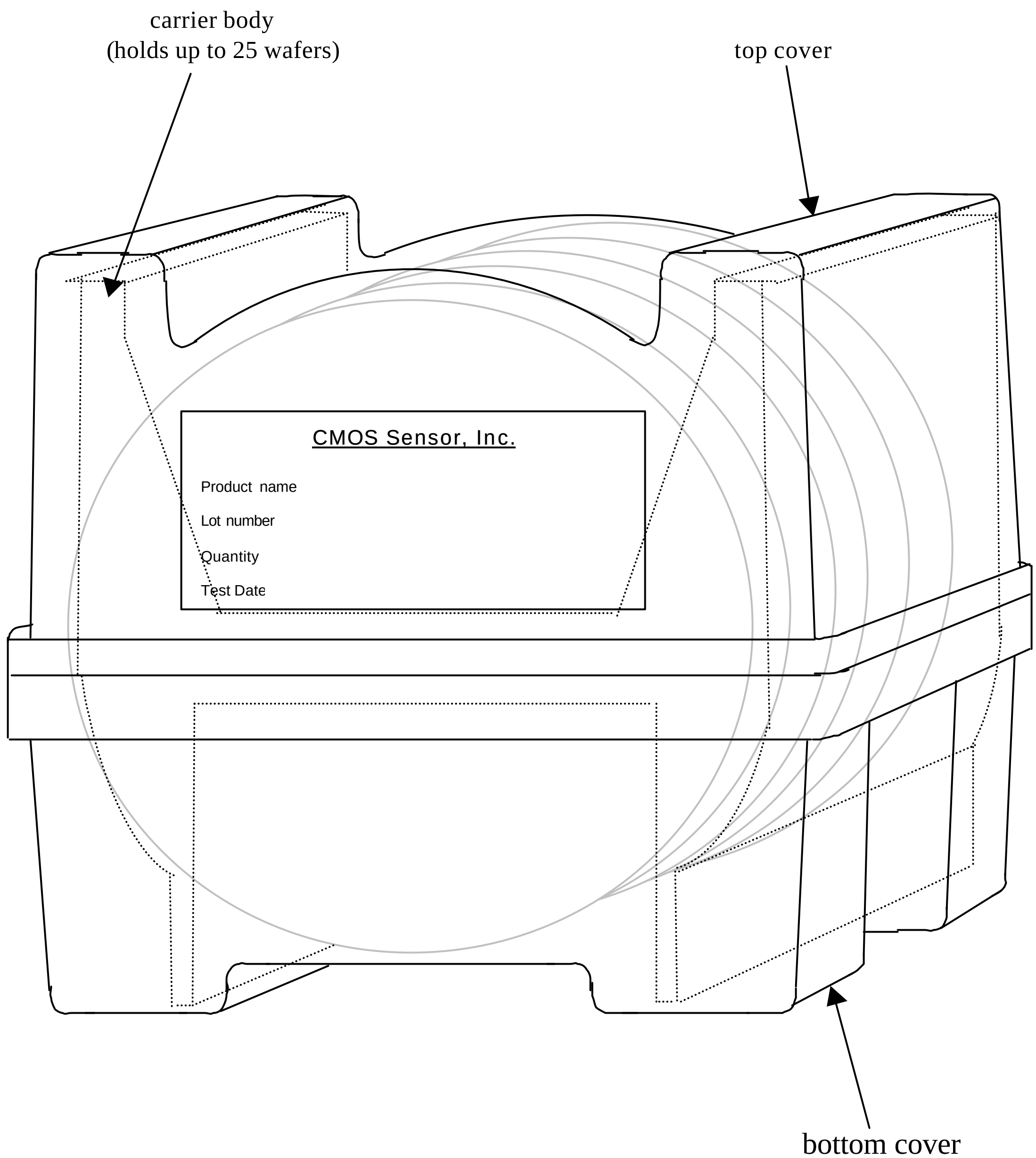
2. Wafers may be shipped in either of two package types:

   (1) a round shipping package.
   (2) a molded wafer shipper.



(repeat paraffin paper and wafer layers up to 100 wafers)

(1) **ROUND SHIPPING PACKAGE**



(2) MOLDED WAFER SHIPPER

2. Identification

A label should be attached to each shipping container.
The label must include the following items:

(1) product name
(2) lot number
(3) quantity
(4) test date

20045 Stevens Creek Blvd., Suite 1A, Cupertino, CA., 95014 USA   Tel: (408) 366-2898; Fax: (408) 366-2698

.