

Preliminary

Linear Image Sensor

Product Name

C118 (200/400 dpi sensor)

Approval		Notes		
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All specifications of this device are subject to change without notice.				

Revision control sheet

Rev	Date	From	Description

C118

PRODUCT SPECIFICATIONS

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Introduction

1. Features:

- High Speed up to 8 MHz Pixel rate
- Sensitivity up to 150 V/Lux-Sec for 400 dpi and 300 V/Lux-sec for 200 dpi.
- 192 x 1 image sensing elements
- 400 dots per inch (dpi) resolution
- 200 dpi / 400 dpi selectable
- 62.5 μm pixel center-to-center spacing
- On-chip timing and clock driver
- On chip OP amplifier
- Very low fixed pattern noise
- Single 5 V or 3.3 V power supply
- 5 V or 3.3 V input signal interface
- One analog output

2. Description:

C118 linear image sensor consists of buffer circuitry, timing generator, shift register, active pixel element array, chip selector, and on-chip differential amplifier. The timing generator provides all the timing circuitry. The active element array consists of 192 active pixel sensors (APS), correlated doubled sampling (CDS) circuitry, and buffer circuitry. The CDS circuitry is made by S/H1 and S/H2 for reset noise cancellation. On chip differential amplifier is used to cancel DC voltage and achieve a very high sensitivity of the analog video output. The on chip differential amplifier is also built-in a power down circuitry that controlled by chip selector to reduce the power consumption. The center to center spacing between two adjacent pixels is 62.5 μm . The photodiodes are parallel-dump and serial-readout devices controlled by a series of active shift registers. The device is easy to operate. In addition to the 5V power supply, only 2 clock signals (input pulse IP and clock pulse input CP) are required to operate this device.

The device is designed for the application of silicon butting contact image sensors. The length of the chip is about 12 mm. One chip can be butted to another chip to form a long image sensor module. The length of the module can be extended to A6, A4, B4, A3, ... up to A0 size. For silicon butting CIS application, the serial data output (EP) of the first chip is connected to the serial data input (SP) of the next chip. The first chip of VDD1 is tied to VDD, the other is tied to ground. In this case, the first 38 clock cycles of the module is used for the dark reference voltage. This device can be used in a wide variety of applications such as counterfeit, check reader, color scanner, digital copier, mark reader, bar code reader, OCR, edge detector, positioning and optical encoding, etc.

Bonding Pad Layout Diagram

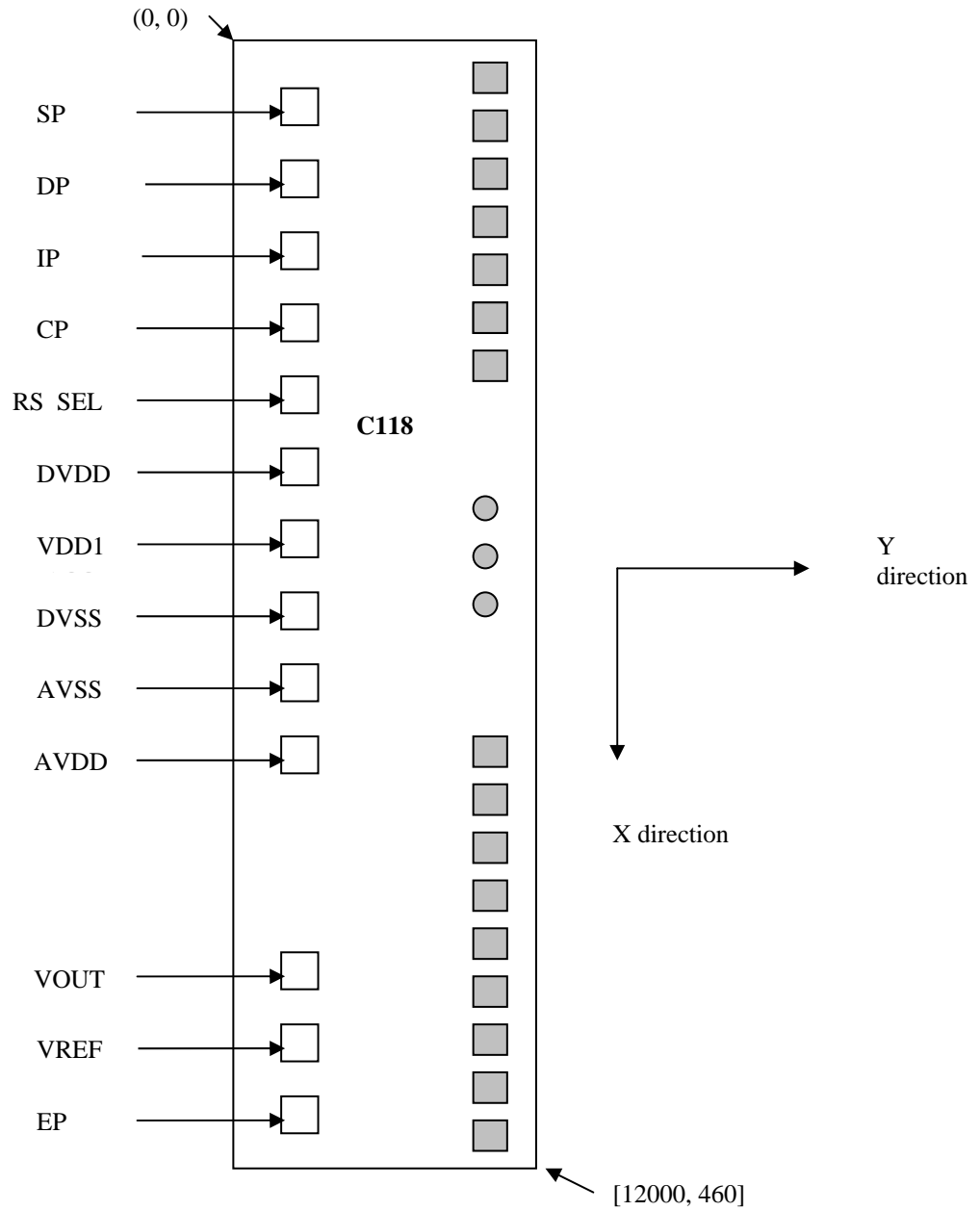


Figure 2. Bonding pad layout diagram

Bonding Pad Description

Pin #	Symbol	Location (x , y) in unit of μm	Description
1	SP	(363, 87)	Start pulse input
2	DP	(738, 87)	Delay pulse output
3	IP	(2982, 87)	Input pulse
4	CP	(3249, 87)	Clock pulse input
5	RS_SEL	(3774, 87)	RS_SEL = 0: 400 dpi RS_SEL = 1: 200 dpi Resolution selectable
6	DVDD	(4136, 87)	Logic power supply; 5 V
7	VDD1	(4394, 87)	To select for first chip
8	DVSS	(46192, 87)	Logic ground; 0 V
9	AVSS	(4902, 87)	Analog ground; 0 V
10	AVDD	(5123, 87)	Analog power supply; 5 V
11	VOOUT	(10857, 87)	Analog (video) signal output
12	VREF	(11243, 87)	Reference voltage input; 1.4 V
13	EP	(11715, 87)	End of pulse output

Table 2. Bonding pad description

Note: Origin: (0 μm , 0 μm) at the left corner of the chip.
 Location: (x μm , y μm) is measured at the center of the pad.
 Pad size: (125 μm by 80 μm)
 Chip size: 400 μm by 12000 μm for the chip without scribe line.
 460 μm by 12060 μm with scribe lines.

Electro-Optical Characteristics

Test conditions:

Measured at $\phi_{\text{CP}} = 1.66 \text{ MHz}$, $V_{\text{DD}} = 5\text{V}$, $t_{\text{int}}^{*(1)} = 0.45 \text{ ms}$, $\lambda^{*(2)} = 565 \text{ nm}$, $\text{Gain}^{*(4)} = 1$,
 $\text{TA}^{*(5)} = 25 \text{ }^\circ\text{C}$, light intensity = 10 LUX.

[See readout circuitry (unless otherwise noted).]

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
	Sensitivity			150		V/lux s
V_{ref}	Reference voltage			1.4		V
f_{CLK}	Clock frequency			3	8	MHz
f_{px}	Pixel rate			3	8	MHz
V_{n}	Random noise			-		mVrms
$V_{\text{c}}^{*(6)}$	Compensated analog output voltage	Light on		1.0		V
$U_{\text{c}}^{*(7)}$	Compensated nonuniformity	Pixel 2 ~ 47**, within a chip	-10	---	+10	%
$U_{\text{p}_5\text{pix}}^{*(8)}$	8 pixel white level nonuniformity	Every 8 pixels, within a chip	-10	---	10	%

$U_{cadj}^{*(9)}$	Compensated adjacent pixel nonuniformity	Within a chip	-10	---	10	%
$C_c^{*(10)}$	Chip-chip compensated nonuniformity	Within a wafer	-15	---	+15	%
$V_d^{*(11)}$	Analog output voltage at dark level	Light off		1.4		V
$U_d^{*(12)}$	Dark signal nonuniformity	Within a chip			100	mV
$C_d^{*(13)}$	Chip-chip dark signal nonuniformity	Within a wafer	---	---	100	mV
	Image lag			0		%

Table 3. Electro-Optical characteristics

Definition:

1. t_{int} is the integration time. It is equal to the interval between two start pulses.
2. λ is the wavelength of the light source.
3. C_{ext} is the off-chip load capacitance for I_{out} .
4. Gain is the gain of an off-chip video operation amplifier.
5. TA is the ambient temperature.
6. $V_c = (V_{cmax} + V_{cmin}) / 2$
where V_{cmax} is the maximum compensated voltage of the whole array.
 V_{cmin} is the minimum compensated voltage of the whole array.
7. U_c is the pixel-to-pixel compensated photo response nonuniformity within a chip.
 $U_c = [((V_{cmax} - V_{cmin})/2) / V_c] \times 100\%$
8. $U_{p_8pix} = \frac{\text{Max}\{\text{Max}[V_p(i), V_p(i+1), \dots, V_p(i+7)] - \text{Min}[V_p(i), V_p(i+1), \dots, V_p(i+7)]\}}{\{\text{Max}[V_p(i), V_p(i+1), \dots, V_p(i+7)] + \text{Min}[V_p(i), V_p(i+1), \dots, V_p(i+7)]\}}$
($i = 1, 2, \dots$)
where $V_p(i)$ is the video signal output of a pixel # i
 $V_p(i+1)$ is the video signal output of a pixel # $(i+1)$
:
:
:
 $V_p(i+7)$ is the video signal output of a pixel # $(i+7)$
9. $U_{cadj} = \text{Max} [|(V_c(i) - V_c(i+1)) / V_c(i)| \times 100\%, (i = 2, 3, \dots, 191)]$
where $V_c(i)$ is the compensated video signal output of a pixel # i
 $V_c(i+1)$ is the compensated video signal output of a pixel # $(i+1)$
10. C_c is the chip-to-chip compensated photo response nonuniformity within a wafer
 $C_c = [(V_c - V_{cavg}) / V_{cavg}] \times 100\%$
where V_{cavg} is the average compensated output signal of all chips within a wafer
11. $V_d = (V_{dmax} + V_{dmin}) / 2$
where V_{dmax} is the maximum dark voltage of the whole array.
 V_{dmin} is the minimum dark voltage of the whole array.
12. $U_d = V_{dmax} - V_{dmin}$
13. C_d is the chip-to-chip dark voltage nonuniformity within a wafer.
 $C_d = V_d - V_{davg}$
where V_{davg} is the average dark voltage of all chips within a wafer.

** Pixel # 1 and # 192 measured by U_{p_8pix}

Absolute maximum ratings:

Power supply voltage, V_{DD}	-----	7 V
Power supply current, I_{DD}	-----	10 mA
Digital input voltage range, V_{ih}	-----	V_{DD}
Digital input current range, I_{ih}	-----	-20 mA to 20 mA
Operating free-air temperature range, T_A	-----	0 °C ~ 50 °C
Storage temperature range, T_{stg}	-----	25 °C ~ 70 °C

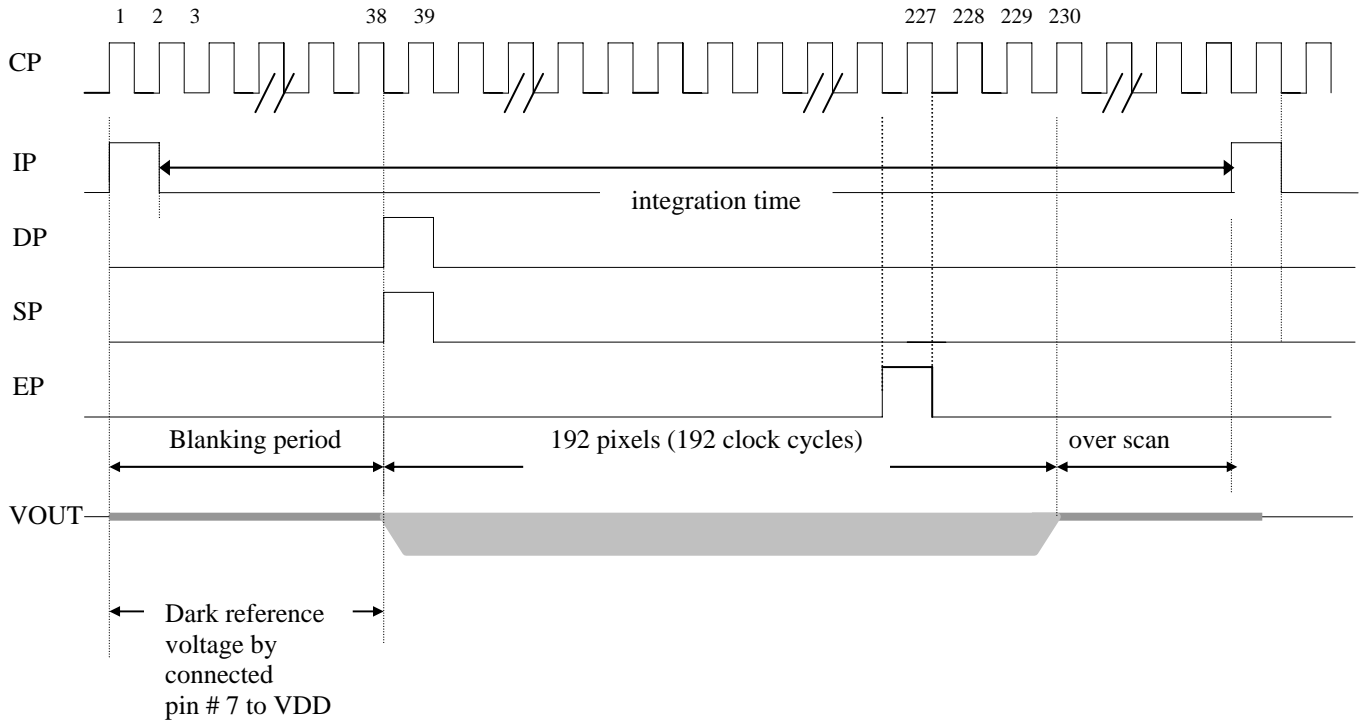
‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended operating conditions:

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.5	5	5.5	V
Power supply current	I_{DD}		3.5		mA
Input voltage	V_i			V_{DD}	V
High level input voltage	V_{ih}	$V_{DD} \times 0.7$		V_{DD}	V
Low level input voltage	V_{iL}	0		$V_{DD} \times 0.3$	V
Clock frequency	f	0.1	3	8	MHz
Sensor integration time	t_{int}		0.1		ms
Wavelength of light source	λ	400		1000	nm
Clock pulse high duty cycle		25	50	75	%
Operating free-air temperature	T_A	0		50	°C

Table 4. Recommended operating conditions.

Timing Diagram (for 400 dpi resolution; RS_SEL = 0)



Timing Diagram (for 200 dpi resolution; RS_SEL = 1)

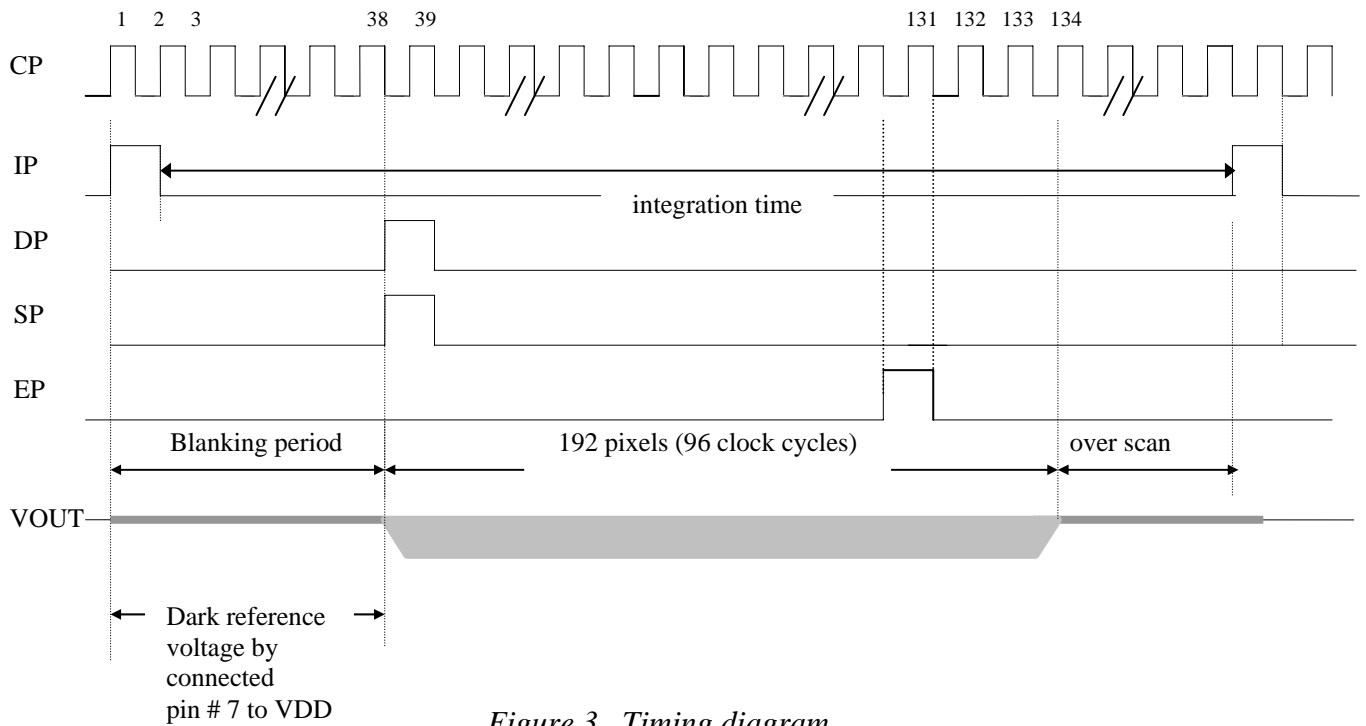


Figure 3. Timing diagram.

Switching Characteristics

Item	Description	Symbol	Min	Typ.	Max	Unit
1	Clock cycle time	t_{oc}		0.5		μs
2	Clock pulse duty cycle: t_w / t_{oc}			50		%
3	Clock pulse width	t_w		100		ns
4	ϕ_{SP} setup time	t_{ss}	50			ns
5	ϕ_{SP} hold time	t_{sh}	50			ns
6	Video digital delay time	t_{pd}		50		ns
8	Video signal stable time	t_s		200		ns

Table 5. Switching characteristics

Switching Waveforms

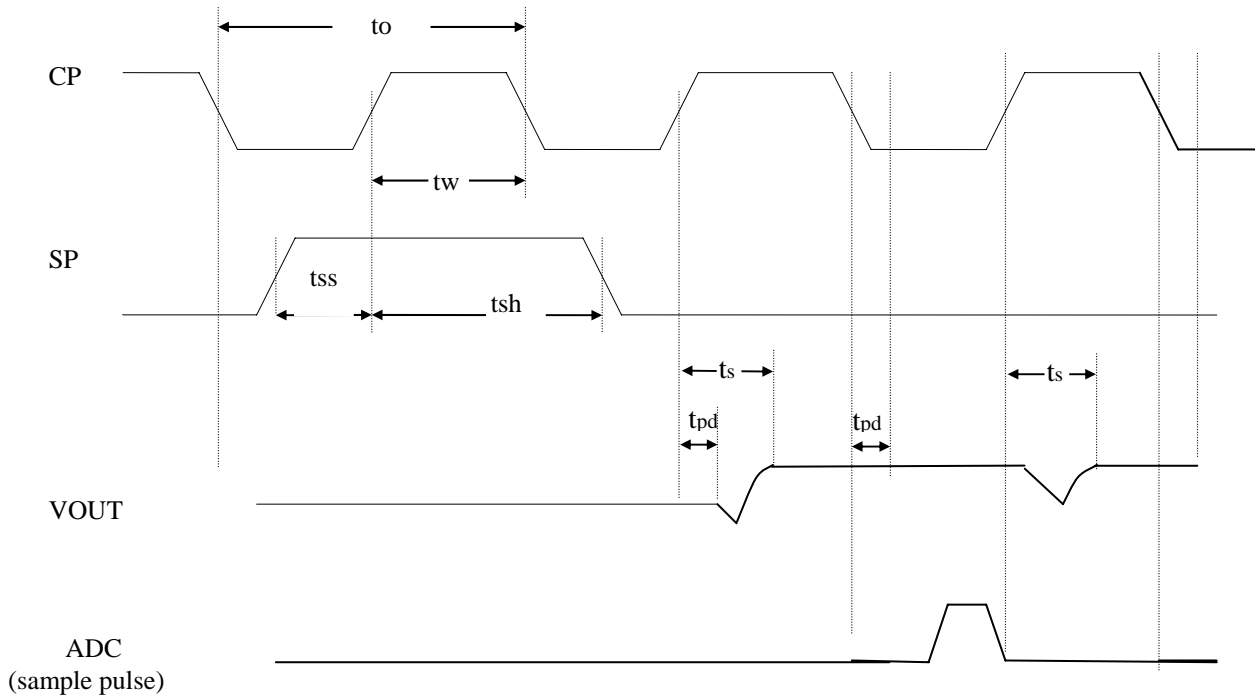


Figure 4. Switching waveforms

CIS Module Schematic

Figure 5 shows the schematic of the Contact Image Sensor (CIS) module using C118 sensor chip. On the first chip, pin 1 is connected to pin 2. On all other chips, pin 2 is floating. The pin # 7 of first chip is connected to VDD, the other chips are connected to Ground. Therefore, the beginning of first 38 clock cycles represents a dark reference voltage on the module. This is used for the dark signal cancellation on the system.

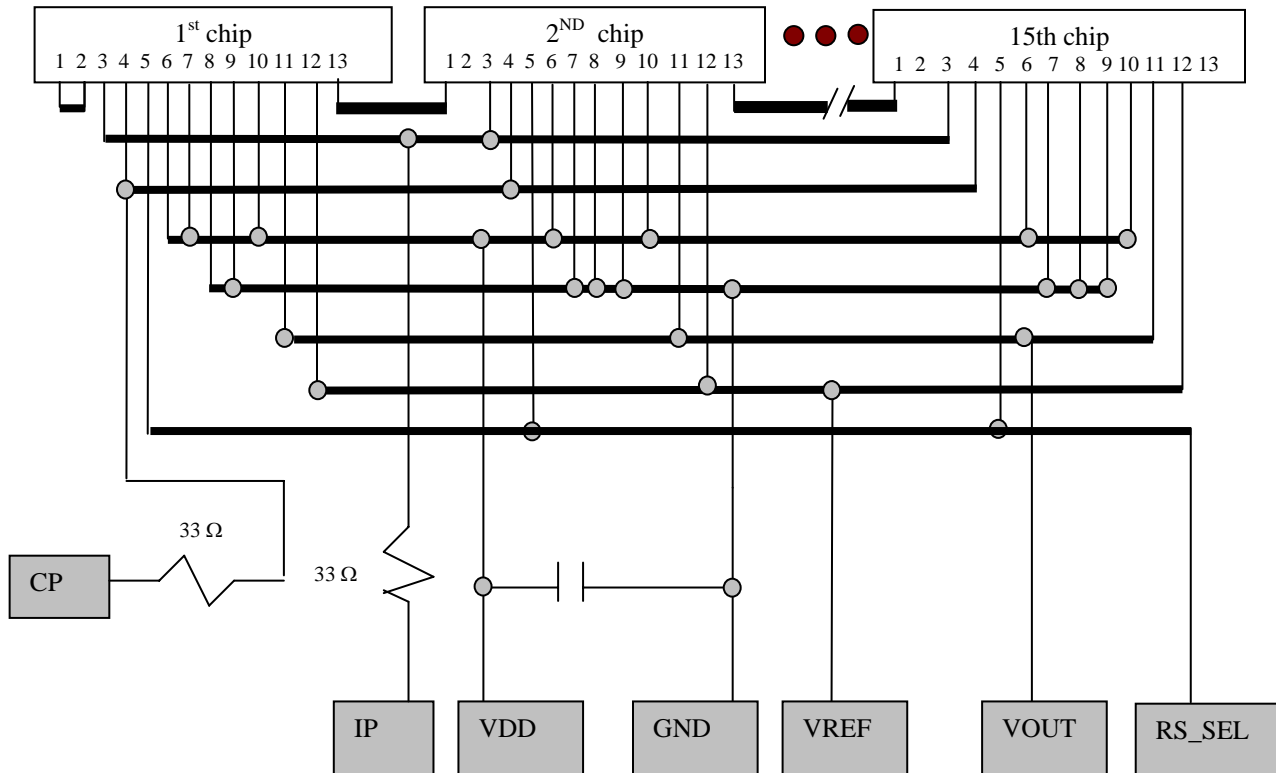
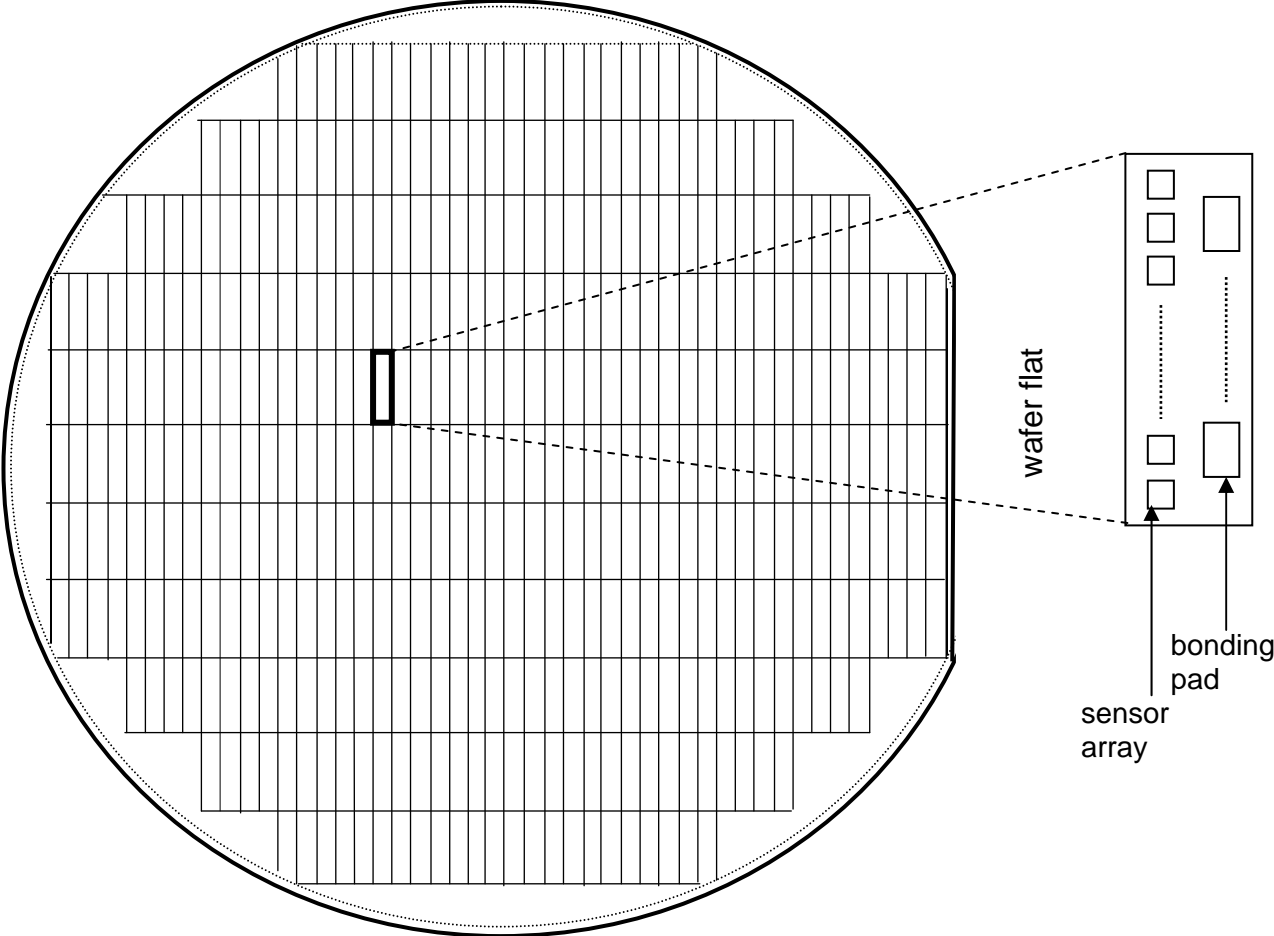


Figure 5. An example of the CIS module schematic.

For module:

Pin # 7 of first chip is connected to VDD, the other is connected to Ground.

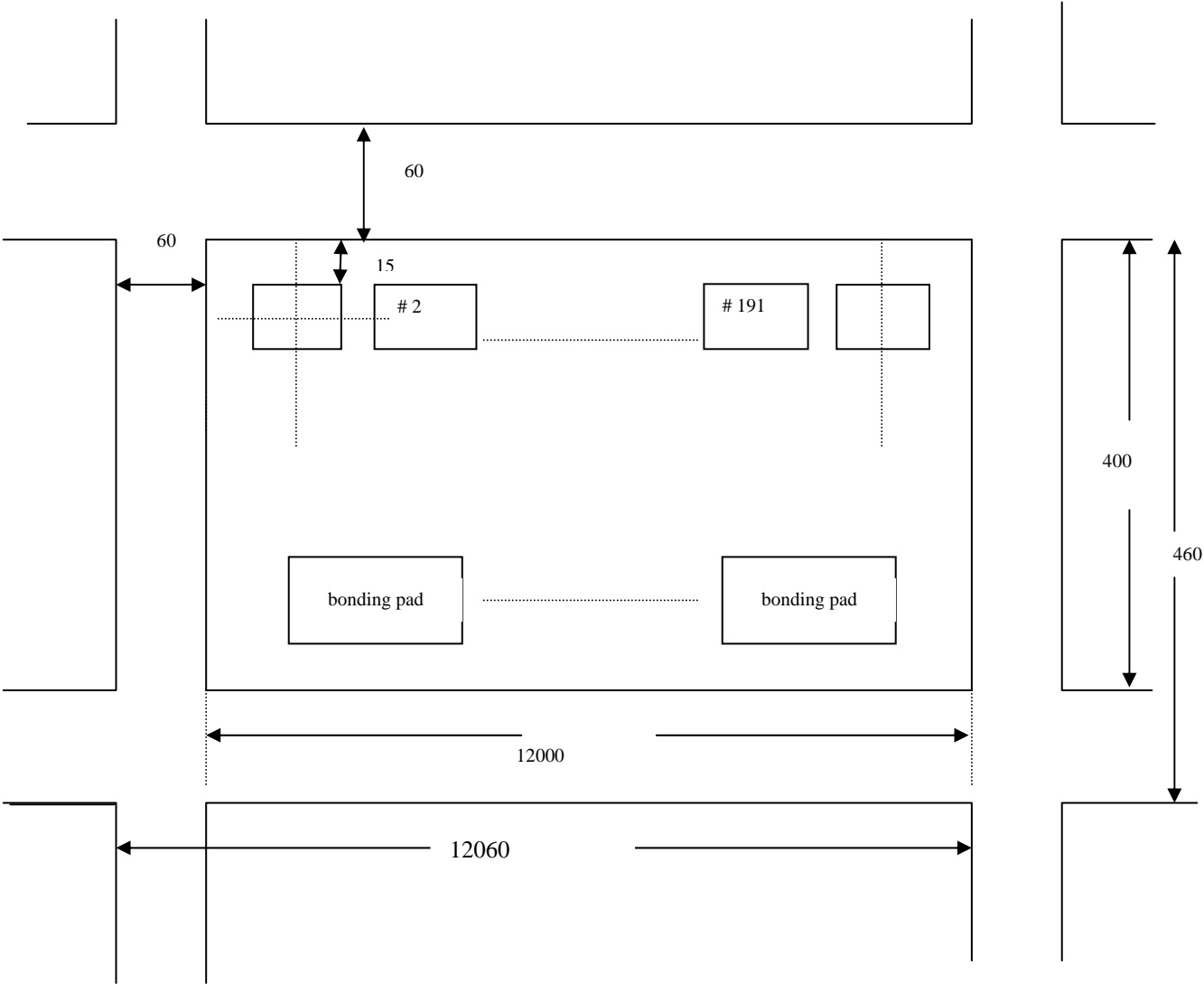
IC Chip Layout on a Wafer



Wafer thickness: 350 μm

Figure 6. Wafer map of C118 chip.

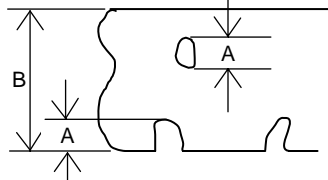
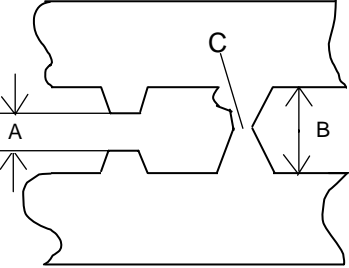
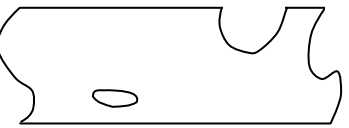
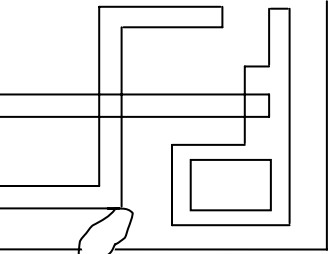
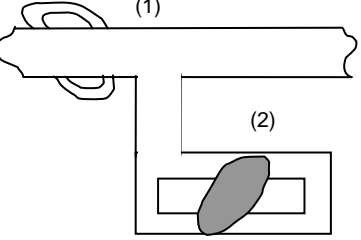
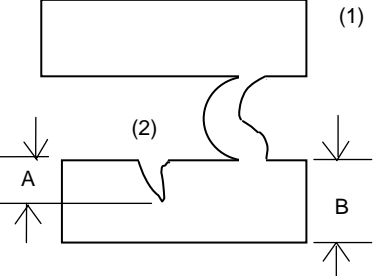
Scribe Line Layout Diagram (unit: micron)

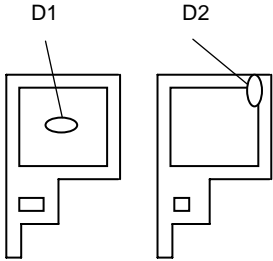
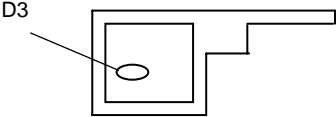
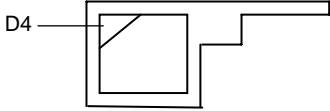
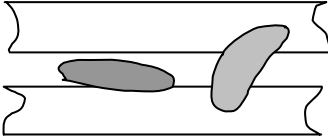
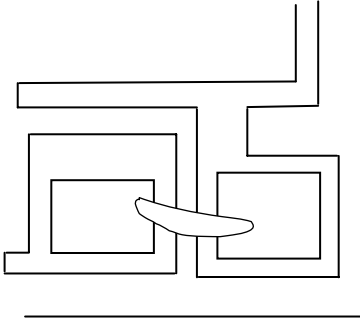
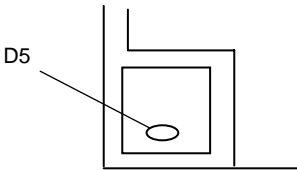


Sensor dimension: 52.5 μm x 52.5 μm

Figure 7. Scribe line layout diagram.

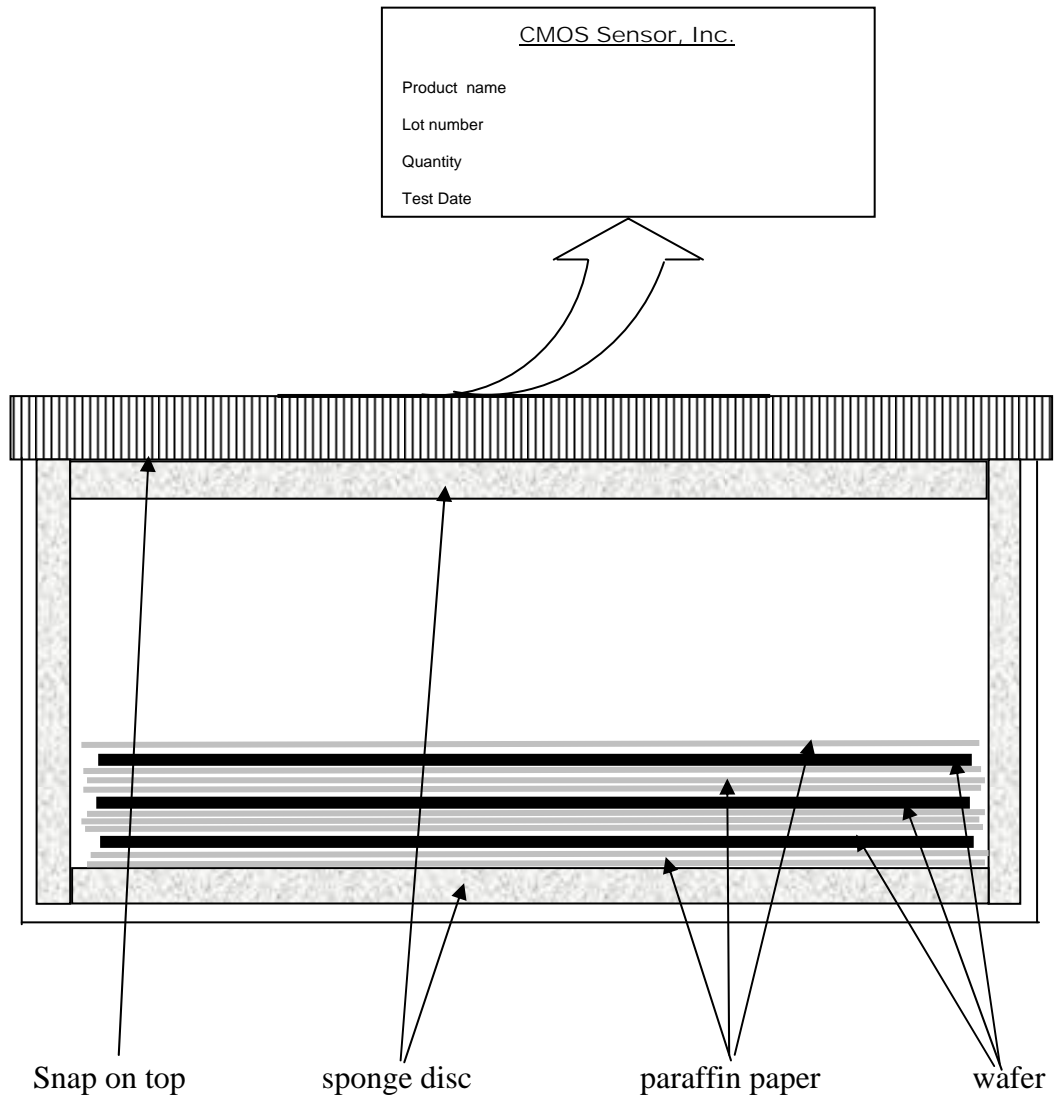
Microscope Inspection Specifications

No.	ITEMS	INSPECTION CRITERION	SIMPLIFIED DIAGRAM
1	BAD METAL LINE	(1) DEFICIENT AND VOID METAL LINE $A \geq B/2$	
		(2) PROXIMITY AND SHORTING OF METAL LINE $A \leq B/2$ C IS SHORTED	
		(3) HILLOCK	
		(4) METAL RESIDUES	
2	BAD OXIDE LAYER	(1) OXIDE LAYER VOID UNDER METAL LINE	
		(2) OXIDE LAYER VOID ON METAL LINE TO THE ACTIVE DEVICE	
3	BAD DIFFUSION	(1) SHORT BETWEEN TWO DIFFUSION REIGONS	
		(2) DEFICIT DIFFUSION REGION $A \geq B/2$	

No.	ITEMS	INSPECTION CRITERION	SIMPLIFIED DIAGRAM
4	BAD BONDING PAD	(1) METAL LAYER VOID EITHER WITHIN PAD OR AT CORNER $D1 \geq D/5$ $D2 \geq D/5$ WHERE D IS THE SIZE OF THE BONDING PAD	
		(2) DISCOLORIZATION OF THE BONDING PAD METAL $D3 \geq D/5$	
		(3) MISSING BONDING PAD METAL	
5	BAD PASSIVATION LAYER	(1) PASSIVATION RESIDUE WITHIN PAD $D4 \geq D/5$ WHERE D IS THE PAD SIZE	
		(2) PASSIVATION VOID ON METAL LINES OR BE- TWEEN METAL LINES	
6	CONTAMINATION AND FOREIGN PARTICLES	(1) CONTAMINATION OR FOREIGN PARTICLE (a) WHICH HAS A SIZE GREATER THAN 50 MICRONS (b) WHICH CONNECTS BETWEEN TWO EXPOSED METAL PATTERNS	
		(2) CONTAMINATION OR FOREIGN PARTICLE ON THE BONDING PAD $D5 \geq D/5$	

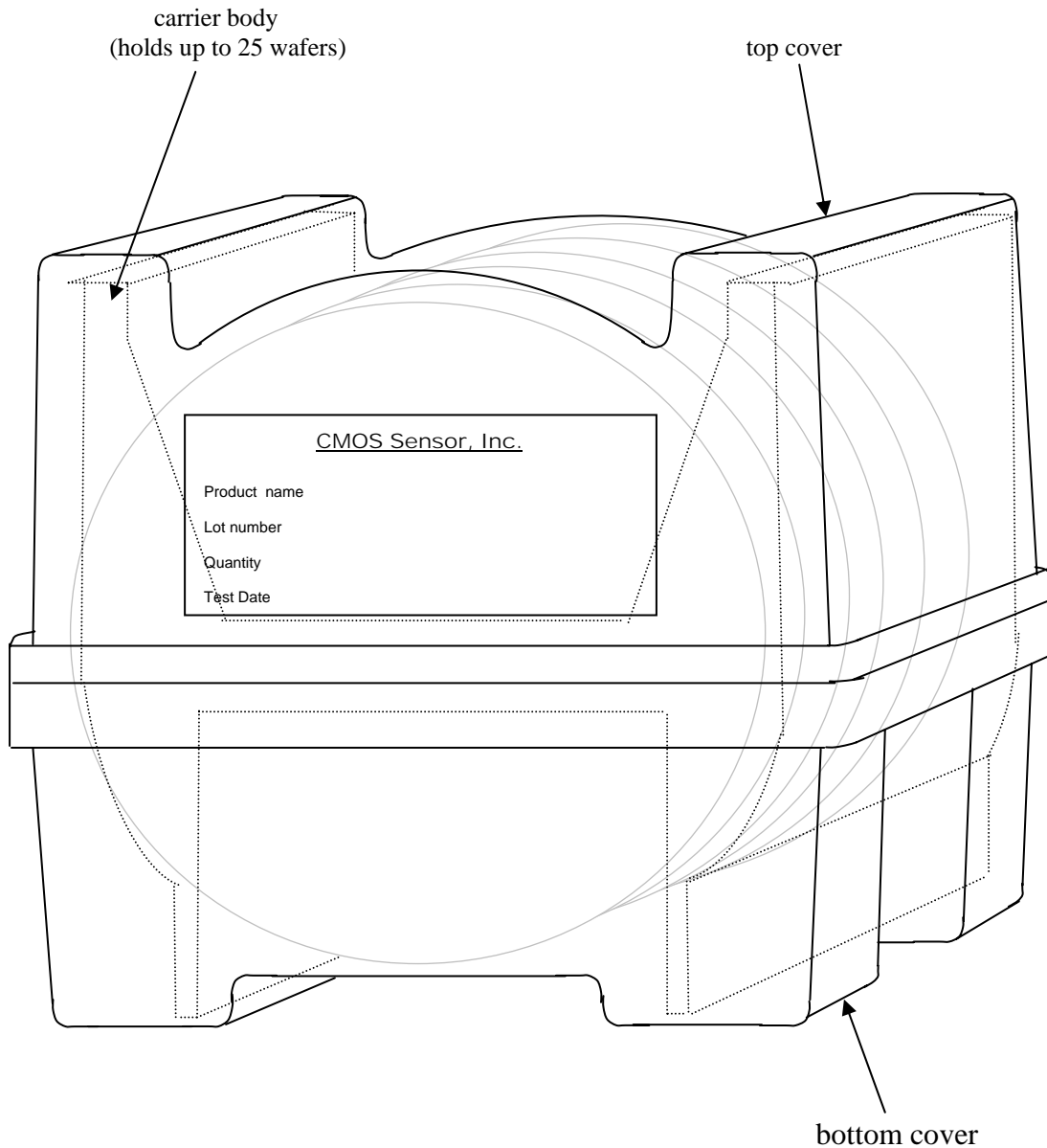
Shipping Package

1. Basically, wafers in the containers shown are manufactured under the same conditions at the same time.
2. Wafers may be shipped in either of two package types:
 - (1) a round shipping package.
 - (2) a molded wafer shipper.



(repeat paraffin paper and wafer layers up to 100 wafers)

(1) ROUND SHIPPING PACKAGE



(2) MOLDED WAFER SHIPPER

2. Identification

A label should be attached to each shipping container.
The label must include the following items:

- (1) product name
- (2) lot number
- (3) quantity
- (4) test date

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