Linear Image Sensor

Product Name	**C106 single chip**

Approval	Notes

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Approved	Checked	Designed

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All specifications of this device are subject to change without notice.

Revision control sheet

Revision No.	Date	Item of change and content	Reason	Approved	Designed

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PRODUCT SPECIFICATIONS

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Introduction

1. Features:
    - 64 x 1 image sensing elements
    - 8 dots per millimeter (dpm) resolution
    - 125 μm pixel center-to-center spacing
    - High sensitivity
    - Internal gain
    - Single 5 V power supply
    - Low power consumption: 10mW maximum
    - Single analog video output signal
    - On-chip analog video switch

2. Description:
   The C106 linear image sensor, about 8 millimeters long, consists of 64 photo detectors, associated multiplexing switches, shift registers, chip selector logic, odd-even circuitry, and analog video switch. Each photo detector is reset more than once during a clock cycle to reduce the image lag. The video signal, which is built in on a chip analog video switch, of the odd photo detector and the even photo detector are combined into one video output signal. The chip selector logic is used to activate the output of the individual chips, making them suitable for silicon butting to form a full width linear Contact Image Sensor (CIS) array. The area of the pixel element is approximately 5400 μm^2 with 125 μm center to center spacing. The photo detectors operate in a serial-dump and serial-readout fashion with a series of active shift registers. The device is easily operated with a start pulse (ϕ_{Sp}), a clock pulse (ϕ_{Cp}), and a single 5V power supply.

   The device is designed for a contact image sensor with the silicon butting technology. These chips can be butted with each other to form a long image sensor module, allowing the length of the module to be extended to A6, A4, B4, A3, ... up to A0 size. Electrically, the start pulse (ϕ_{Sp}) of the second chip is connected to the end of pulse (ϕ_{Ep}) of the first chip, etc. This device can also be used in a wide variety of applications including mark readers, bar code readers, OCR, edge detectors, positioning and optical encoding.

Functional Block Diagram

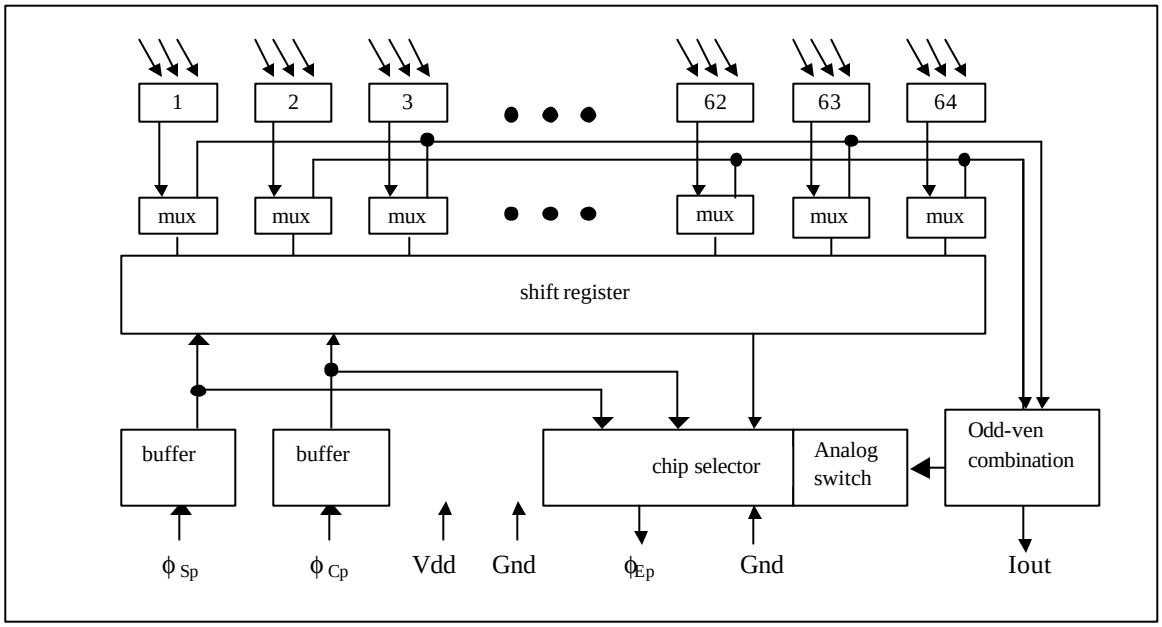

Figure 1. Functional Block Diagram

Package Layout Diagram

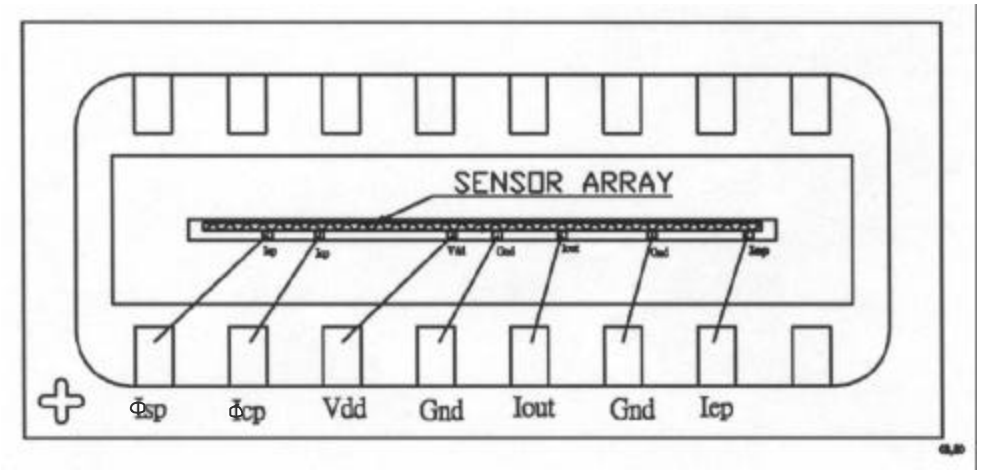

Figure 2. Single chip package layout diagram

Terminal Description

Terminal Number	Symbol	Name	Description
1	ϕ_{Sp}	Start pulse terminal	To apply a pulse to start signal integration
2	ϕ_{Cp}	Clock pulse terminal	To apply an external clock pulse to chip
3	Vdd	Positive power supply terminal	To connect + 5 V normally
4	Gnd	Ground terminal	To connect to 0 V normally
5	Iout	Video signal output terminal	Send the photo current signal out
6	Gnd	Ground terminal	Connected to pin # 4 inside the chip
7	ϕ_{Ep}	End of pulse terminal	Send a pulse to indicate an end of scan
8	NC	No connection	
9 ~ 16	NC	No connection	

Table 1. Terminal Description

Electro-Optical Characteristics

Test conditions:
Measured at ϕ_{Cp} = 500 kHz, Vdd = 5V, t_{int} $^{*(1)}$ = 2 ms, $\lambda^{*(2)}$ = 565 nm, C_{ext} $^{*(3)}$ = 47 pF, Gain$^{*(4)}$ = 2,
TA$^{*(5)}$ = 25 °C, light intensity = 7.2 LUX.
[See readout circuitry (unless otherwise noted).]

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_c $^{*(6)}$	Compensated analog output voltage	Light on	400	700	1000	mV
U_c $^{*(7)}$	Compensated nonuniformity	Pixel 2 ~ 63**, within a chip	-10	---	+10	%
U_{p_5pix} $^{*(8)}$	5 pixel white level nonuniformity	Every 5 pixels, within a chip	-7.5	---	7.5	%
U_{cadj} $^{*(9)}$	Compensated adjacent pixel nonuniformity	Within a chip	-7	---	7	%
C_c $^{*(10)}$	Chip-chip compensated nonuniformity	Within a wafer	-13	---	+13	%
V_d $^{*(11)}$	Analog output voltage at dark level	Light off	-200	---	+100	mV
U_d $^{*(12)}$	Dark signal nonuniformity	Within a chip	---	---	100	mV
C_d $^{*(13)}$	Chip-chip dark signal nonuniformity	Within a wafer	---	---	200	mV
I_{dd}	Power supply current		---	---	2	mA

Table 2. Electro-Optical characteristics

Definition:

1. t_{int} is the integration time, which is equal to the interval between two start pulses.
2. λ is the wavelength of the light source.
3. C_{ext} is the off-chip load capacitance for $I_{out.}$
4. Gain is the gain of an off-chip video operation amplifier.
5. TA is the ambient temperature.
6. Vc = (Vcmax + Vcmin) / 2
   where Vcmax is the maximum compensated voltage of the whole array.
   Vcmin is the minimum compensated voltage of the whole array.
7. Uc is the pixel-to-pixel compensated photo response nonuniformity within a chip.
   Uc = [((Vcmax - Vcmin)/2) / Vc] x 100%
8. U_{p_5pix} = Max {Max[(Vp(i), Vp(i+1), …, Vp(i+4)] – Min[(Vp(i), Vp(i+1), …, Vp(i+4)]} / {Max[Vp(i), Vp(i+1),…,Vp(i+4)]+Min[(Vp(i), Vp(i+1),…,Vp(i+4)]}
   (i = 1, 2, …, 60)
   where Vp(i) is the video signal output of a pixel # i
   Vp(i+1) is the video signal output of a pixel # (i+1)
   :
   :
   Vp(i+4) is the video signal output of a pixel # (i+4)
9. Ucadj = Max [|(Vc(i) - Vc(i+1)| / Vc(i)] x 100%, (i = 2, 3, …, 63)
   where Vc(i) is the compensated video signal output of a pixel # i
   Vc(i+1) is the compensated video signal output of a pixel # (i+1)
10. Cc is the chip-to-chip compensated photo response nonuniformity within a wafer
    Cc = [(Vc - Vcavg) / Vcavg] x 100%
    where Vcavg is the average compensated output signal of all chips within a wafer
11. Vd = (Vdmax + Vdmin) / 2
    where Vdmax is the maximum dark voltage of the whole array.
    Vdmin is the minimum dark voltage of the whole array.
12. Ud = Vdmax – Vdmin
13. Cd is the chip-to-chip dark voltage nonuniformity within a wafer.
    Cd = Vd - Vdavg
    where Vdavg is the average dark voltage of all chips within a wafer.

** Pixel # 1 and # 64 measured by $Up_{\_5pix}$

Absolute Maximum Rating

Power supply voltage, Vdd ---------- 7 V
Power supply current, Idd ---------- 2 mA
Digital input voltage range, Vih ----------Vdd
Digital input current range, Iih ---------- - 2 mA to + 2 mA
Operating free-air temperature range, Ta ---------- 0 ℃ ~ 50 °C
Storage temperature range, Tstg ---------- - 25 °C ~ 70 °C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under " recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Item	Symbol	Min	Typ.	Max	Unit
Power supply voltage	Vdd	4.5	5	5.5	V
Power supply current	Idd			2	mA
Input voltage	V_i			Vdd	V
High level input voltage	V_{ih}	4		Vdd	V
Low level input voltage	V_{iL}	0		0.8	V
Clock frequency	f	5	500	3000	kHz
Sensor integration time	t_{int}		2.5		ms
Wavelength of light source	λ	400		700	nm
Clock pulse high duty cycle		25	50	75	%
Operating free-air temperature	Ta	0		50	°C

Table 3. Recommended operating Conditions

Timing Diagram

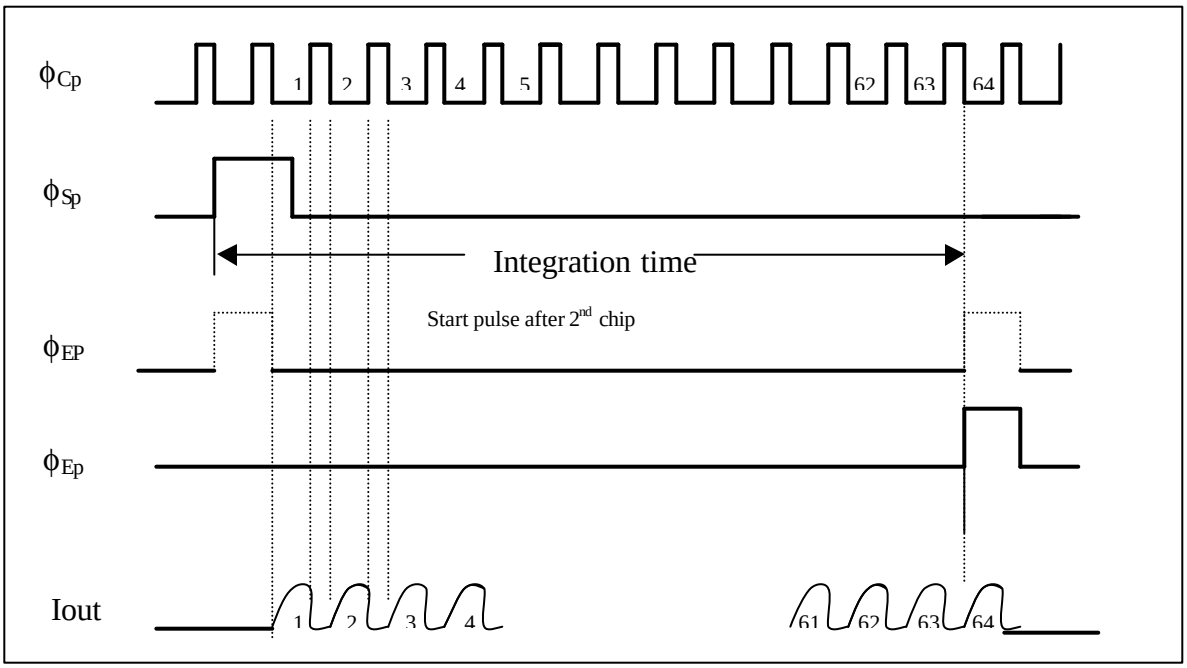

Figure 3. Timing diagram

Readout Circuitry

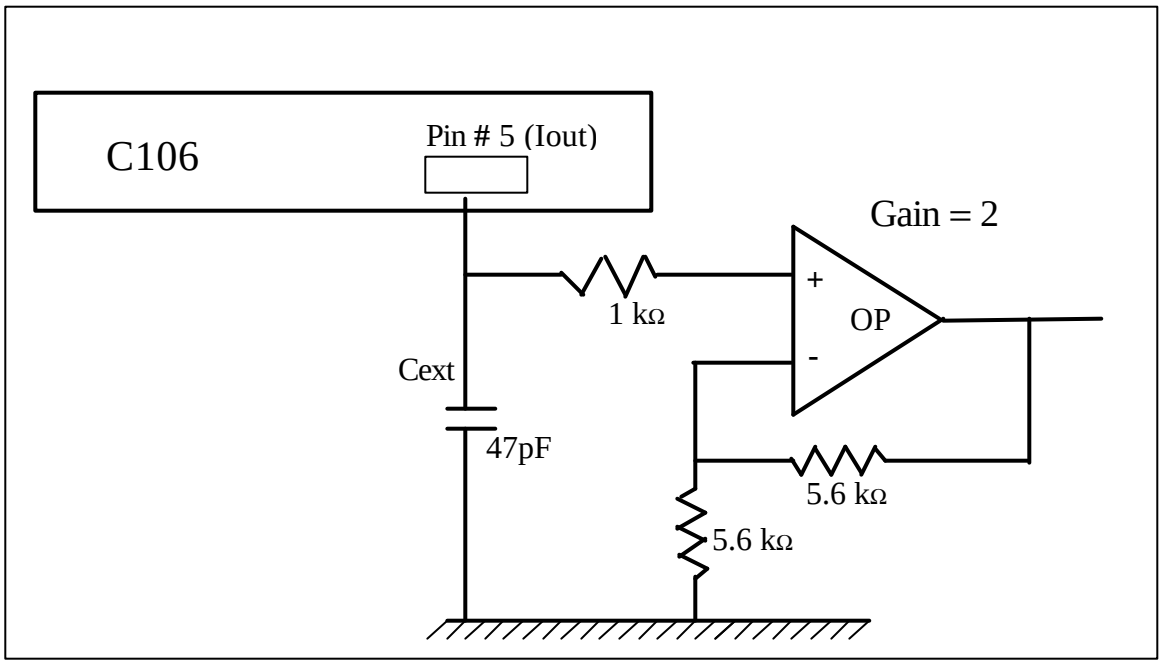

Figure 4. Readout circuitry

Switching Characteristics

Item	Description	Symbol	Min	Typ.	Max	Unit
1	Clock cycle time	to		2		μs
2	Clock pulse duty cycle: tw / to			25		%
3	Clock pulse width	tw		500		ns
4	ϕ_{Sp} setup time	tss	50			ns
5	ϕ_{Sp} hold time	tsh	50			ns
6	Video digital delay time	td		68	800	ns
7	Video signal invalid time	ti		25		ns
8	Video signal stable time	ts	36			ns

Table 4. Switching characteristics

Switching Waveforms

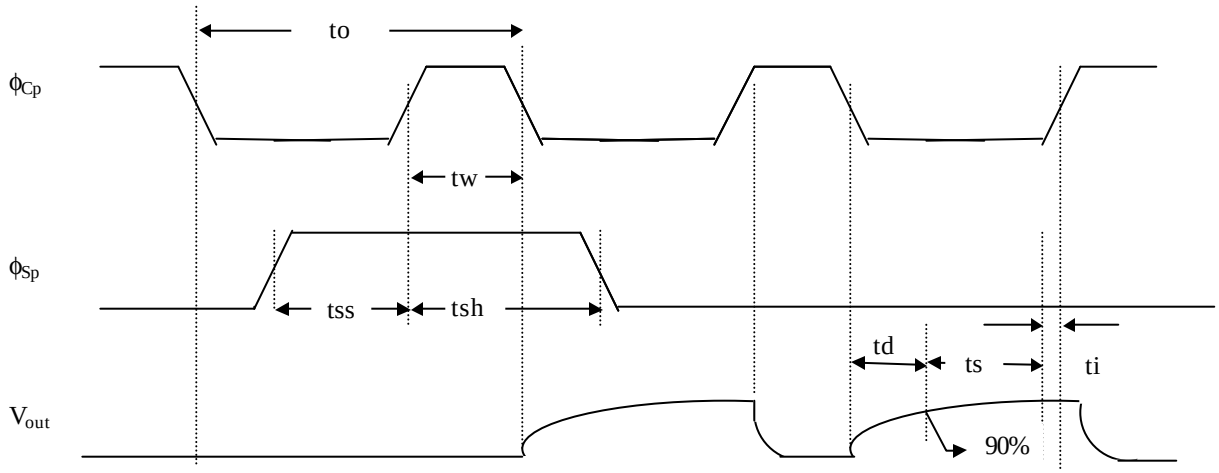

Figure 5. Switching waveforms